Synchronization Architectures for Legacy Video Integrated Circuits and Modern CCTV Display Interfaces

1. Introduction: The Convergence of Disparate Video Timing Domains

The integration of vintage microelectronics with industrial surveillance display technology presents a distinct and complex set of signal integrity challenges, primarily centered on the synchronization of time-bases. The technical query at hand involves the interface between a General Instrument AY-3-8500 "Ball & Paddle" integrated circuit—or substantially similar legacy analog Charge-Coupled Device (CCD) camera hardware—and a professional Closed-Circuit Television (CCTV) monitor. The reported symptom, described as the input signal failing to lock to the monitor's oscillator and running out of phase, is a classic manifestation of frequency domain incompatibility between a free-running source and a mains-referenced sink.

This phenomenon is not merely a matter of cabling or connector mismatches but touches upon the fundamental architectural differences between consumer video game design of the mid-1970s and the rigorous standards of the security video industry. The consumer device relies on a "slave" display that adapts to the source, whereas the industrial monitor acts as a "master," expecting the source to conform to an external reference. This report provides an exhaustive technical analysis of these interoperability issues, exploring the theoretical underpinnings of composite video generation in NMOS logic, the physics of Cathode Ray Tube (CRT) and Liquid Crystal Display (LCD) synchronization, and the operational mechanics of Phase-Locked Loops (PLL).

Furthermore, this document investigates the feasibility of "injecting sync" into the AY-3-8500. It posits that while direct injection of a synchronization pulse into the video output path is electrically invalid, the objective can be achieved through the construction of an active Genlock circuit. This involves modulating the chip's master clock input using a PLL referenced to the AC mains zero-crossing point, effectively slaving the vintage silicon to the modern power grid.

2. Theoretical Framework: The Physics of Analog Video Synchronization

To fully comprehend the synchronization failure between an AY-3-8500 and a CCTV monitor, one must first dissect the fundamental principles of analog video timing and the distinct

architectural decisions made by engineers in the 1970s versus those in the security industry. The video signal is a time-domain representation of a two-dimensional image, and its stability relies entirely on the precise alignment of time-bases between the generating device and the display device.

2.1 The Composite Video Signal Architecture

The standard NTSC or PAL video signal is a complex waveform combining luminance (brightness), chrominance (color), and synchronization information into a single channel. The AY-3-8500, introduced in 1976, generates a simplified version of this standard, often non-interlaced (progressive), which was sufficient for the tolerance of 1970s domestic television sets but often violates the strict timing expectations of professional video equipment.[1]

Synchronization pulses are "negative" voltage excursions (typically 0V or below the black level) that instruct the display when to return the electron beam (or digital raster pointer) to the start of a line (Horizontal Sync) or the top of the screen (Vertical Sync). In a standard broadcast environment, these pulses are derived from extremely precise master generators, often atomic clocks or thermally stabilized crystal ovens. In the low-cost AY-3-8500, they are derived via integer division from a single master clock, nominally 2.0 MHz.[2]

Parameter	NTSC Standard	PAL Standard	AY-3-8500 (Approx)
Lines per Field	262.5	312.5	262 (NTSC) / 312 (PAL)
Field Rate	59.94 Hz	50.00 Hz	Variable (LC Oscillator)
Line Frequency	15.734 kHz	15.625 kHz	~15.625 kHz
Sync Voltage	-40 IRE (0.3V)	0.3V below Black	0V (Rail to Rail Logic)

The critical deviation here is the field rate. A professional NTSC signal is exactly 59.94 Hz. A PAL signal is exactly 50.00 Hz. The AY-3-8500, driven by a cheap inductor-capacitor (LC) oscillator, may drift anywhere from 55 Hz to 65 Hz depending on temperature and voltage.[3]

2.2 The "Line Lock" Phenomenon in CCTV Systems

CCTV monitors and cameras were historically designed with a specific constraint not present

in home broadcasting: the need to switch video signals using a sequential switcher without the picture "rolling" or "bouncing".[5]

If two cameras are free-running, their vertical sync pulses will occur at random times relative to each other. When a switcher cuts from Camera A to Camera B, the monitor receives a vertical sync pulse at an unexpected time. The monitor's deflection circuits (or frame buffer) must re-lock to this new timing. In a CRT, this involves the physical magnetic collapse of the yoke field, a process that takes milliseconds. Visually, this results in the image jumping or rolling vertically for a second or two before stabilizing.[6]

To mitigate this, the security industry adopted **Line Lock (LL)**. Since all cameras in a building are typically powered by the same AC mains utility, the AC voltage frequency (60Hz in North America, 50Hz in Europe) provides a ubiquitous, common reference clock. By synchronizing the vertical interval of every camera to the zero-crossing point of the AC mains, all cameras generate vertical sync pulses simultaneously.[6]

The CCTV monitor, when set to "Line Lock," expects the incoming video signal's vertical sync to be phase-aligned with the AC mains. If an AY-3-8500 game is connected, its internal oscillator runs at a frequency determined by local components. Even if this frequency is exactly 60.00Hz (which is statistically improbable for an LC circuit), it will not be *phase-locked* to the wall outlet powering the monitor. The resulting beat frequency manifests as a horizontal bar rolling slowly up or down the screen.[5]

2.3 The "Free-Running" Architecture of AY-3-8500

The General Instrument AY-3-8500 is a masterpiece of optimization for its era. It uses a single master clock input on **Pin 17** to drive all internal logic.[7] The datasheet specifies a nominal frequency of 2.0 MHz (specifically 2.012160 MHz for NTSC).[7]

Internally, binary ripple counters divide this 2 MHz signal to generate the requisite timing signals:

1. **Pixel Clock:** 2 MHz (500ns per pixel).
2. **Horizontal Sync:** 2 MHz / 128 ≈ 15.625 kHz.
3. **Vertical Sync:** Horizontal / 262 (NTSC) or 312 (PAL) ≈ 60Hz or 50Hz.[2]

Crucially, the chip has no "Sync Input" pin to reset these counters. The **Reset (Pin 25)** only resets the game score and state logic (e.g., ball position, score counters), not the video raster counters.[7] Therefore, the chip cannot be traditionally "genlocked" by simply sending it a reset pulse at the start of every frame. The only way to synchronize the AY-3-8500 to an external source (like the AC mains) is to **control the speed of the master clock on Pin 17**.

This represents a fundamental divergence from the user's hypothesis of "injecting sync." One

cannot inject sync into an output; one must modulate the time-base that generates the sync.

3. Comprehensive Analysis of the AY-3-8500 Integrated Circuit

Before engineering a solution, we must characterize the electrical and logical properties of the subject device. The AY-3-8500 is an NMOS (N-channel Metal-Oxide Semiconductor) device, which dictates specific power supply and interfacing logic requirements distinct from modern CMOS or TTL.

3.1 Power and Logic Levels

Unlike modern TTL (5V) or CMOS (3.3V) logic, the AY-3-8500 operates optimally at **+6V to +7V**, with a maximum rating of +12V.[2] Standard 5V logic levels may arguably drive the inputs, but reliable operation often requires level shifting or a dedicated 6-7V supply.[4]

- **Logic '0':** 0V to 0.5V.
- **Logic '1':** $V_{cc} - 2V$ to V_{cc}.

This high "Logic 1" threshold (e.g., 4V minimum on a 6V supply) implies that standard 3.3V microcontrollers cannot drive Pin 17 directly without buffering.[7] Any Genlock circuit designed must respect these voltage domains to avoid damaging the vintage silicon or failing to trigger the clock input.

3.2 Pinout Functionality Relevant to Synchronization

Understanding the pinout is critical for identifying injection and extraction points for the synchronization loop.

Pin	Name	Direction	Function	Significance for Sync
16	Sync Output	Output	Combined H-Sync and V-Sync	Open-drain output requiring pull-up/mixing resistors. This is the **Feedback** source for any PLL circuit.[12]

17	Clock Input	Input	Master Timebase (2.0 MHz)	The **Control** point. The only way to change the video timing is to vary the frequency injected here.[2]
24	Score/Field	Output	Video Data (Luminance)	Must be mixed with Pin 16 to form composite video.[7]
6, 9, 10	Ball/Player	Output	Video Data (Luminance)	Independent video layers mixed via resistor ladder.[8]
25	Reset	Input	Game Logic Reset	Resets scores, not raster timing.[7]
3	Sound Output	Output	Audio pulses	Frequency is derived from the Master Clock, so audio pitch will shift if the clock is modulated.[7]

3.3 The Native Oscillator Instability

The standard application note circuit for the AY-3-8500 uses a simple LC (Inductor-Capacitor) oscillator or a crude logic gate oscillator.

- **LC Circuit:** A tank circuit connected between pins, relying on a specific inductance (often hand-wound). This is notoriously unstable, drifting with temperature and supply voltage.[3]
- **Drift Implications:** If the clock drifts by even 0.1%, the vertical frequency shifts. A monitor in "Internal" mode might track this (using its own PLL), but a monitor in "Line

Lock" mode will see a massive phase error. The vertical hold will fail, and the image will roll.

4. Diagnostics: Analyzing the User's Problem

The user states: *"the input signal does not lock on the oscillator in the monitor so they run out of phase."* This phrasing is technically precise. The monitor has a local oscillator (deflection driver) and the game has a local oscillator (Pin 17). They are running at slightly different frequencies ($f_1 \neq f_2$) and possess no phase coherency ($\phi_1 \neq \phi_2$).

4.1 Symptom 1: Rolling Picture

If the monitor is set to Line Lock (referencing 60Hz AC), and the AY-3-8500 is running at 59.9Hz or 60.1Hz (due to an imperfect 2.0MHz oscillator), the vertical blanking interval of the game will drift relative to the monitor's retrace cycle.

- **Visual Manifestation:** A black horizontal bar (the vertical sync interval) moves vertically through the image.
- **Cause:** Beat frequency between f_{mains} and f_{game}. The speed of the roll is directly proportional to the frequency difference.

4.2 Symptom 2: Tearing / Flagging

If the horizontal frequency is unstable or far out of spec (e.g., 16kHz instead of 15.625kHz), the monitor's horizontal flywheel circuit may fail to lock.

- **Visual Manifestation:** The top of the picture skews to the side (flagging) or the image breaks up into diagonal lines.
- **Cause:** The monitor's Horizontal Phase-Locked Loop (HPLL) has a limited capture range (typically ± 500 Hz). If the AY-3-8500 oscillator is too far off (e.g., wrong inductor value), the monitor simply cannot lock.

4.3 Symptom 3: Line Lock ("LL") vs Internal ("INT")

Professional CCTV monitors almost always feature a synchronization switch, often physical (on the back) or in a digital menu.

- **INT (Internal):** The monitor ignores the mains phase and locks purely to the sync pulses embedded in the incoming video signal (Pin 16 of AY-3-8500). This is how consumer TVs work.
- **LL (Line Lock):** The monitor ignores the timing of the incoming vertical sync pulses and forces its vertical scan to align with the AC mains. If the video source isn't also locked to mains, the picture rolls.[14]

The user's description strongly suggests the monitor is in **LL** mode, or the monitor is defective

and its sync separator is failing to extract the non-standard sync from the game.

5. Solution Pathway A: Monitor-Side Configuration (The Non-Invasive Fix)

Before attempting complex circuit modifications, the most robust solution is to reconfigure the display device. The user's query implies the monitor "normally does its own sync," which strongly suggests it is defaulted to Line Lock mode.

5.1 Locating the Sync Switch

In professional CRT and LCD CCTV monitors (e.g., JVC, Pelco, Sony, Panasonic), this setting is ubiquitous.

- **Physical Switches:** Look for a slide switch on the rear panel labeled SYNC with options INT and LL.[16]
- **DIP Switches:** On older chassis or "camclosure" units, this may be a DIP switch on the board (e.g., Pelco IS90 series uses SW4-3).[18]
- **OSD Menu:** Modern LCD CCTV monitors often bury this in the SYSTEM or SETUP menu under SYNC MODE.[19]

5.2 The "INT" Mode

By setting the monitor to **INT** (Internal), the monitor behaves like a standard television. It extracts the sync pulses from the composite video signal provided by the AY-3-8500 (Pin 16) and locks its local deflection oscillators to *that* signal.

- **Result:** The rolling stops immediately. Even if the AY-3-8500 clock drifts, the monitor will track it (within reasonable limits).

Recommendation: This is the primary solution. However, if the user *must* use Line Lock (e.g., the monitor is part of a larger system that requires it, or the switch is broken/absent), we must explore Source-Side modifications.

6. Solution Pathway B: Source-Side Stabilization (Crystal Oscillator)

If the AY-3-8500 is using the original LC oscillator (coil and capacitor), its frequency stability is poor. A simple "drift" might be confusing the monitor's sync separator, even in INT mode.

6.1 Crystal Oscillator Implementation

Replacing the LC circuit with a quartz crystal provides a frequency stability of roughly $\pm$

20-50 ppm, compared to the $\pm$5-10% of an LC circuit.

- **Target Frequency:** 2.012160 MHz (NTSC) or 2.000000 MHz (PAL).[7]
- **Circuit:** A Pierce oscillator using a CMOS inverter (e.g., CD4069 or CD4001) is the standard approach.[4]

Circuit Diagram Description:

1. **IC:** CD4069UB (Unbuffered Hex Inverter).
2. **Crystal:** 2.0 MHz connected between Input (Pin 1) and Output (Pin 2).
3. **Feedback Resistor:** 1MΩ to 10MΩ parallel to the crystal to bias the inverter into the linear region.[22]
4. **Load Capacitors:** Two 22pF-33pF capacitors from each leg of the crystal to Ground.[23]
5. **Output:** Pin 2 of the CD4069 feeds Pin 17 (Clock Input) of the AY-3-8500.

Limitations: While this creates a *stable* frequency, it is still **not phase-locked** to the wall mains. If the monitor remains in Line Lock mode, the image will still roll, albeit at a very constant, predictable speed. This solution only fixes issues if the monitor is in INT mode but struggling with a jittery source.

7. Solution Pathway C: "Injecting Sync" via Phase-Locked Loop (PLL)

This section addresses the user's specific hypothesis: *"maybe it is possible to inject sync back into the video game?"*

As established, the AY-3-8500 has no "Sync In" pin. However, we can "inject" synchronization by creating a **Genlock** system. This involves dynamically adjusting the 2.0 MHz clock frequency so that the generated Vertical Sync aligns perfectly with the AC Mains zero-crossing. This is a classic application for a **Phase-Locked Loop (PLL)**.

7.1 The Architecture of a Mains-Locked PLL

We require a circuit that multiplies the 60Hz (or 50Hz) mains frequency up to 2.0 MHz.

- **Target Multiplier (NTSC):** $2,012,160 \text{ Hz} / 60 \text{ Hz} = 33,536$.
- **Target Multiplier (PAL):** $2,000,000 \text{ Hz} / 50 \text{ Hz} = 40,000$.

This division ratio is extremely high for a single loop, potentially leading to jitter. However, since the vertical timing is derived from the clock by a fixed integer ($128 \times 262 = 33,536$), locking the vertical interval is mathematically equivalent to locking the clock.

7.2 Component Selection: The CD4046

The **CD4046** Micropower Phase-Locked Loop is the industry standard for this task.[11] It contains:

1. **VCO (Voltage Controlled Oscillator):** Can generate 2 MHz.
2. **Phase Comparators:** Compare the reference signal phase to the feedback signal phase.

7.3 Circuit Design: The Genlock Loop

To lock the AY-3-8500 to the mains, we construct the following loop:

1. **Reference Signal (Mains):**
   - Extract a low-voltage AC signal from the power supply transformer (before rectification).
   - Pass this through a Schmitt Trigger (e.g., CD4093 or CD40106) to create a clean 50/60Hz square wave.[26]
   - This is fed into **Pin 14 (Signal In)** of the CD4046.
2. **Feedback Signal (Video Sync):**
   - Take the **Sync Output (Pin 16)** from the AY-3-8500.
   - This pin outputs *composite* sync (containing both Horizontal and Vertical pulses).
   - We need to isolate the **Vertical Sync** (60Hz) to compare it with the mains.
   - **Sync Separator:** Use an **LM1881** Video Sync Separator. Input the AY-3-8500 composite video/sync; Output Pin 3 is **Vertical Sync**.[28]
   - Feed this Vertical Sync into **Pin 3 (Comparator In)** of the CD4046.
3. **VCO (The Master Clock):**
   - The CD4046 VCO (Pin 4) output is connected to the AY-3-8500 **Clock Input (Pin 17)**.
   - **Frequency Setting:** Components $R1$, $R2$, and $C1$ on the CD4046 must be selected to center the VCO frequency at 2.0 MHz.
     - $C1 \approx 100pF$.
     - $R1 \approx 10k\Omega - 50k\Omega$.
   - The AY-3-8500 divides this 2 MHz down to 60Hz internally.
4. **Closing the Loop:**
   - The CD4046 compares the *Mains 60Hz* (Reference) with the *AY-3-8500 Vertical Sync* (Feedback).
   - If the game is running too fast (Sync arriving before Mains), the Phase Comparator outputs an error voltage.
   - This voltage is filtered (Low Pass Filter) and fed to the VCO Control (Pin 9).
   - The VCO slows down. The game clock slows down. The Vertical Sync aligns with the Mains.
   - **Result:** The AY-3-8500 is now "Line Locked."

7.4 Feasibility and Challenges

- **Jitter:** The AY-3-8500 generates sync based on digital counters. The mains frequency is relatively "sloppy" and analog. The PLL loop filter must be overdamped to prevent the video clock from jittering excessively, which would cause horizontal shaking (flagging).[30]
- **Sync Separation:** The AY-3-8500 sync output is non-standard logic levels. The LM1881 requires a standard video level (1Vpp). You may need to attenuate the Sync Output from the AY-3-8500 (logic level 6V) down to ~1V before feeding the LM1881.[28]
- **Complexity:** This is a non-trivial circuit requiring an oscilloscope to tune the lock range.

8. Solution Pathway D: Analog CCD Camera Synchronization

The user also mentions an "old analog CCD camera." This is a simpler case because many professional analog cameras have built-in external sync capabilities.

8.1 External Sync Inputs

Check the back of the CCD camera for connectors labeled:

- **LL / INT Switch:** Just like the monitor, the camera might have a switch. Set it to **LL** to lock it to the mains, matching the monitor.
- **V-Phase Adjustment:** If set to LL, there is often a potentiometer labeled "V-Phase".[6] This allows you to delay the vertical sync pulse relative to the mains zero-crossing. Adjust this while watching the monitor until the rolling stops or the vertical interval switching is clean.
- **Genlock / Sync In:** High-end cameras (e.g., JVC, Sony, Panasonic) have a BNC connector labeled SYNC IN, GENLOCK, or VBS IN.
    - **Action:** You can feed a "Black Burst" or "Composite Sync" signal here.
    - **Master Generator:** In a studio, a master sync generator feeds all cameras. In a standalone fix, you could use a simple sync generator chip (like an SAA1043 or simpler logic) to drive both the camera (if it supports ext sync) and the monitor (if it supports ext sync).

8.2 Modifying Cameras without External Sync

If the camera is a cheap consumer module (e.g., board cam) with only Video Out, Power, and Ground:

- It is likely strictly internal crystal controlled.
- **Solution:** You *cannot* line-lock this camera. You *must* set the monitor to INT (Internal Sync).
- **Alternative:** Use a "Time Base Corrector" (TBC). A TBC digitizes the incoming instable video into a frame buffer and outputs a perfectly stable, retimed video signal. This is the professional (albeit expensive) solution to mix free-running sources.[32]

9. Circuit Implementation Guide: The "Injector" Circuit

For the user wishing to build the PLL Genlock for the AY-3-8500, here is the synthesized component specification.

9.1 Required Components

- **PLL IC:** CD4046BE (CMOS Phase Locked Loop).
- **Sync Separator:** LM1881N.
- **Logic Gates:** CD40106 (Schmitt Trigger Inverter) for mains conditioning.
- **AY-3-8500:** The target device.
- **Power Supply:** 6V Regulated (Critical for AY-3-8500 stability).

9.2 Schematic Connectivity

1. **Mains Reference:**
   - Transformer Secondary (e.g., 9V AC) $\rightarrow$ 10k Resistor $\rightarrow$ CD40106 Input (Pin 1).
   - CD40106 Output (Pin 2) $\rightarrow$ CD4046 Signal In (Pin 14).
2. **VCO Output:**
   - CD4046 VCO Out (Pin 4) $\rightarrow$ AY-3-8500 Clock In (Pin 17).
3. **Feedback Path:**
   - AY-3-8500 Sync Out (Pin 16) $\rightarrow$ 470Ω Series Resistor $\rightarrow$ 1kΩ Pull-down to GND (to simulate video load) $\rightarrow$ 0.1μF Capacitor $\rightarrow$ LM1881 Video In (Pin 2).
   - LM1881 Vert Sync Out (Pin 3) $\rightarrow$ CD4046 Comparator In (Pin 3).
4. **Loop Filter (Between Pin 13 and Pin 9 of CD4046):**
   - Series Resistor ($R3$): 10kΩ.
   - Capacitor to Ground ($C2$): 1μF (Start large to dampen jitter).
   - **Note:** Use Phase Comparator II (Pin 13) for edge-triggered logic, which is better for this digital locking than the XOR gate of Comparator I.[25]

10. Detailed Engineering Addendum: Composite Video Mixing and Buffering

While synchronization is the primary issue, signal integrity is a frequent secondary point of failure in these projects. The AY-3-8500 outputs separate signals for Ball, Players, and Field. These must be mixed to create a composite signal the monitor can accept.

10.1 The Resistor Ladder Mixer

The datasheet suggests summing the outputs using resistors. For a 75Ω system (CCTV standard), the high-impedance outputs of the AY-3-8500 are insufficient.

- **Sync (Pin 16):** Strongest pull-down. Requires lowest resistor value.
- **Video (Pins 6, 9, 10, 24):** Higher resistor values for different grey levels (Luma).

Recommended Mixing Values (for 2N3904 Buffer Input):

- Sync (Pin 16) $\rightarrow$ 3.3kΩ
- Ball/Player (Pins 6,9,10) $\rightarrow$ 1kΩ (White)
- Field/Score (Pin 24) $\rightarrow$ 2.2kΩ (Grey)
- Common Point $\rightarrow$ Base of NPN Transistor.

10.2 The Output Buffer

CCTV monitors present a 75Ω termination load. Connecting the mixing resistors directly will attenuate the signal to near zero.

- **Circuit:** NPN Emitter Follower (e.g., 2N2222 or 2N3904).
- **Collector:** To Vcc (+6V).
- **Base:** To Mixing Point.
- **Emitter:** To Video Output (RCA/BNC) AND a 470Ω resistor to Ground.
- **Coupling:** A 220μF capacitor in series with the output is recommended to block DC bias, though many CCTV monitors have internal AC coupling.[33]

By ensuring the signal amplitude is correct (~1Vpp) and the impedance is low, the monitor's sync separator (in INT mode) will have the best chance of holding a stable image.

11. Advanced Implementation: Building the PLL Genlock Circuit

For the enthusiast or engineer committed to the "injection" solution (Solution Pathway 3), this section details the practical construction of the PLL Genlock. This is a non-trivial circuit, but it represents the "Gold Standard" for integrating vintage electronics into professional broadcast or security environments.

11.1 Circuit Block Diagram

The topology required is a **Frequency Multiplier PLL**. We are taking a 60Hz reference and multiplying it by ~33,536 to get ~2.012 MHz.

Block 1: The Mains Interface (Reference)

- **Goal:** Safe extraction of the zero-crossing timing.
- **Safety Warning:** NEVER connect logic directly to high-voltage mains (120V/240V). Always tap from the *secondary* side of the step-down transformer (e.g., the 9V AC line before it hits the rectifier bridge).
- **Component:** CD40106 Hex Schmitt Trigger.
- **Circuit:**
  - Input: 9V AC from transformer.
  - Series Resistor: 100kΩ (to limit current).
  - Clamping Diodes: The CD40106 inputs have internal clamping diodes to Vcc and Vss, but external Schottky diodes (e.g., 1N5817) are safer to clamp the AC sine wave to the 0-7V logic rails.
  - Schmitt Action: The CD40106 cleans the sine wave edges into a sharp 60Hz square wave.

Block 2: The Feedback Path (Vertical Sync Extraction)

- **Goal:** Extracting the 60Hz vertical pulse from the AY-3-8500.
- **Component:** LM1881 Video Sync Separator.
- **Input Conditioning:** The AY-3-8500 Sync Output (Pin 16) is a logic-level signal (0V to +Vcc). The LM1881 expects a standard composite video signal (0.3V sync tip, 0.7V video).
  - *Attenuator:* Use a voltage divider. Connect Pin 16 to a 4.7kΩ resistor. Connect the other end to the LM1881 Input (Pin 2). Connect a 560Ω resistor from Pin 2 to Ground. This roughly simulates a video level signal.
  - *Coupling:* Use a 0.1μF capacitor in series with Pin 2 to DC-block the signal.
- **Output:** Pin 3 (Vertical Sync Output) of the LM1881 provides a clean, active-low pulse corresponding to the vertical interval. Invert this (using a spare gate on the CD40106) if the PLL Comparator expects a positive edge (though CD4046 Comparator II is edge-sensitive and versatile).

Block 3: The Phase Locked Loop (CD4046)

- **VCO Configuration (Pins 6, 7, 11, 12):**
  - We need a center frequency (f_0) of roughly 2 MHz.
  - Using the datasheet nomographs for the CD4046 at Vcc=6V:
    - $C1$ (Pin 6-7) = 100 pF.
    - $R1$ (Pin 11) = 22 kΩ.
    - This should allow the VCO to sweep from <1MHz to >3MHz, easily covering the target.
- **Phase Comparator (Pins 3, 14, 13):**
  - **Signal In (Pin 14):** 60Hz from Mains Interface.
  - **Comparator In (Pin 3):** 60Hz Vertical Sync from Feedback Path.

    - **Phase Comparator II Out (Pin 13):** This output is a tri-state logic signal. It pumps up/down pulses to charge/discharge the loop filter capacitor. It is crucial to use Comparator II (not I) because Comparator I (XOR) requires a 50% duty cycle on both inputs to lock at the center of the range. The vertical sync pulse is very narrow (duty cycle < 5%), so Comparator II is mandatory.
- **Loop Filter (Pins 13 to 9):**
    - The loop bandwidth must be very low (e.g., < 10 Hz). We want the clock to drift slowly to match the mains, not jitter on every cycle.
    - $R3$ (Series): 100 kΩ.
    - $C2$ (Filter Cap): 1 μF to 10 μF (Tantalum or high-quality Electrolytic).
    - *Note:* A large time constant here ensures the picture is stable. If the time constant is too fast, the 2 MHz clock will modulate with the 60Hz ripple, causing "curving" or "flagging" at the top of the screen.

Block 4: Injection

- **VCO Out (Pin 4):** Connect directly to AY-3-8500 Pin 17.

11.2 Calibration and Testing

1. **Open Loop Test:** Disconnect the feedback path. Measure the frequency at CD4046 Pin 4. Adjust $R1$ (or a trim pot in series with it) until the frequency is naturally sitting around 2.0 MHz with the control voltage (Pin 9) at $Vcc/2$.
2. **Close Loop:** Connect the feedback. Monitor Pin 9 (VCO Control Voltage) with a scope or multimeter.
    - It should settle to a stable DC voltage.
    - If it oscillates (voltage swinging up and down), increase the Loop Filter capacitor ($C2$).
3. **Visual Check:** Connect the video output to the CCTV monitor in **Line Lock** mode. The rolling bar should stop and hold steady.

12. Alternative Solution: The LM1881 "Overlay" Method (Sync Replacement)

If building a PLL is too complex, there is a "cheat" method often used in video overlay circuits that might satisfy the user's need to stop the rolling, provided they can modify the video path significantly.

12.1 Concept: Sync Stripping and Insertion

Instead of locking the *source* to the *monitor*, we can strip the "bad" sync from the AY-3-8500

and insert "new" sync that the monitor likes. *However*, this is fundamentally flawed for a game console.

- The game logic (ball position, paddles) is tied to the *original* sync timing.
- If you strip the sync and insert new sync (e.g., from a mains-locked generator), the game image will drift relative to the new sync.
- **Result:** The picture will roll *inside* the monitor frame. The monitor will have stable sync, but the game graphics will scroll vertically.
- **Conclusion:** This method works for static cameras where you can just "time base correct" the signal, but for a generated signal like a game, **you must control the generator clock**. The PLL method (Section 7) is the only valid approach.

13. Dealing with Legacy Analog CCD Cameras

The user query also mentions "old analog CCD camera." The solution matrix for cameras is distinct because cameras often have features the AY-3-8500 lacks.

13.1 The "Line Lock" Switch on Cameras

Professional analog cameras (Pelco, Panasonic, Bosch) almost always have a synchronization switch.

- **INT:** Crystal controlled. Use this if your monitor is in INT mode or if you have a single camera.
- **LL:** Line Lock. Use this if you have a switcher and multiple cameras.
    - *Critical Adjustment:* **V-PHASE**. Because 3-phase power is common in large buildings, the "zero crossing" at the camera's outlet might be 120 degrees out of phase with the "zero crossing" at the monitor's outlet.
    - The **V-PHASE** potentiometer on the camera adds a delay (0 to ~16ms) to the sync generation. You simply turn this knob until the camera's vertical interval aligns with the switcher's interval.

13.2 Genlock Input

If the camera has a BNC connector labeled **GENLOCK** or **VBS IN**:

- This is the superior synchronization method.
- It accepts a "Black Burst" signal (a video signal with no picture, just sync and color burst).
- If you have a source of stable sync (e.g., a master sync generator), feed it here. The camera will slave its internal pixel clock and frame timing to this signal.

14. Conclusion

The synchronization mismatch between the AY-3-8500 and the CCTV monitor is a solvable engineering challenge. The root cause is the monitor's **Line Lock (LL)** expectation

encountering a free-running source.

1. **Primary Recommendation:** Attempt to switch the monitor to **Internal (INT)** sync mode. This is the zero-cost, non-invasive solution that respects the design intent of both devices.
2. **Secondary Recommendation:** If Line Lock is mandatory, constructing a **PLL Genlock** using a CD4046 and LM1881 is the only technically valid method to "inject sync" into the AY-3-8500. This circuit slaves the game's master clock to the mains frequency, satisfying the monitor's phase requirements.
3. **For Analog Cameras:** Utilize the onboard **LL/INT** switches and **V-Phase** adjustments inherent to professional CCTV hardware.

This analysis confirms that while the AY-3-8500 is a relic of the mid-1970s, its simple clock-driven architecture allows for sophisticated modern retrofitting (via PLL), bridging the gap between vintage gaming and industrial surveillance standards.

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