BP5758D

Five-channel High-voltage Dimmable Linear LED Driver

Description

The BP5758D is a five-channel high-precision dimmable constant-current linear LED driver. It is targeted for tunable warm/cold/color smart lighting application.

The BP5758D integrates five-channel (OUT1/2/3/4/5) 500V/90mA MOSFET. It achieves output current adjustment with 1024 gray-scale level and eliminates flicker during dimming process.

The BP5758D integrates thermal regulation function to reduce output current at hot temperature, make the system reliable and prevent overheating.

The BP5758D is available in ESOP-8 package.

ESOP8

Features

- Five channels with separate control
- Integrated with 90mA/500V MOSFET for each channel
- Independent maximum output current setting for each channel
- 1024 gray-scale level output current adjustment for each channel
- I2C controlled for smart dimming
- Ultralow quiescent current with 100uA in sleep mode
- ±4% LED output current
- Thermal regulation function
- Available in ESOP-8 package

Applications

- Smart LED bulbs
- Smart filament LED bulbs
- Other smart LED lamps

Typical Application

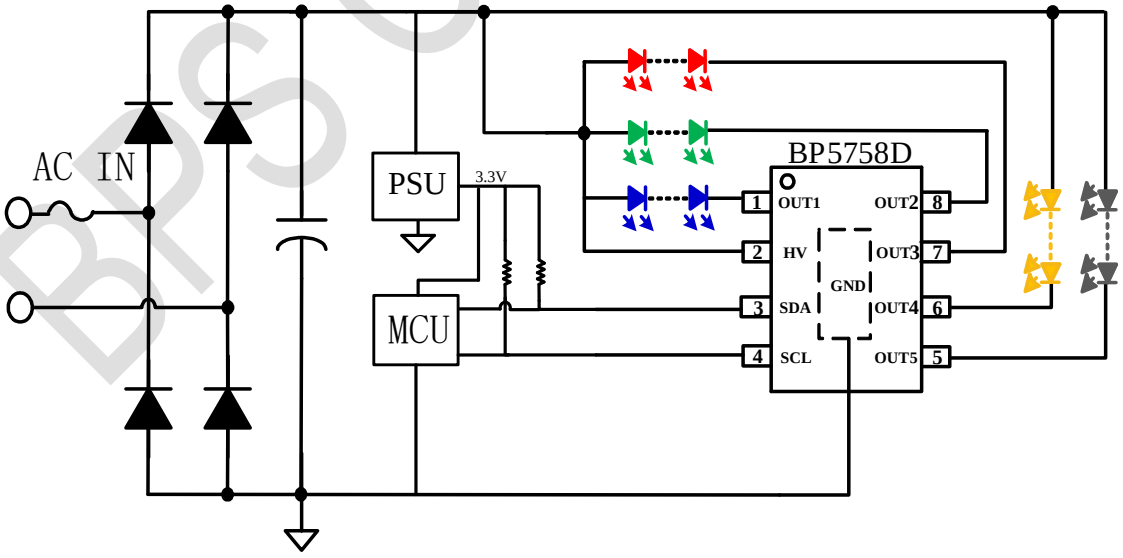
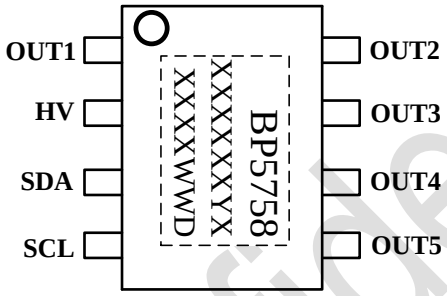


Figure1. BP5758D Typical Application

Ordering Information

Part Number	Package	Temperature	Package Method	Marking
BP5758D	ESOP-8	-40°C ~105°C	Tape 4,000 pcs/Reel	BP5758 XXXXXXYX XXXXWWD

Pin Configuration and Marking Information



BP5758：Part number
XXXXXXY: Lot code
XXXX: Sign
WW: Week

Figure 2: Pin configuration

Pin Definition

Pin NO.	Name	Description
1	OUT1	Constant current output pin 1 (Blue recommended)
2	HV	High voltage power supply input pin
3	SDA	Data input pin (1kΩ external pull-up resistor to Vcc required)
4	SCL	Clock input pin (1kΩ external pull-up resistor to Vcc required)
5	OUT5	Constant current output pin 5 (Cold-white recommended)
6	OUT4	Constant current output pin 4 (Warm-white recommended)
7	OUT3	Constant current output pin 3 (Red recommended)
8	OUT2	Constant current output pin 2 (Green recommended)
Exposed Pad	GND	Ground

Absolute Maximum Ratings (Note 1,2)

Symbol	Parameters	Range	Units
OUT1/2/3/4/5	OUT1/2/3/4/5 pin voltage	-0.3~500	V
IOUT1/2/3/4/5_MAX	OUT1/2/3/4/5 pin current	90	mA
HV	High voltage power supply input pin	-0.3~500	V
SDA	Data input pin	-0.3~9	V
SCL	Clock input pin	-0.3~9	V
P_{DMAX}	Power dissipation (note2)	1.25	W
θ_{JA}	Thermal resistance (Junction to Ambient)	100	°C/W
TJ	Operating junction temperature	-40 to 150	°C
TSTG	Storage temperature range	-55 to 150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Under "recommended operating conditions" the device operation is assured, but some particular parameter may not be achieved. The electrical characteristics table defines the operation range of the device, the electrical characteristics is assured on DC and AC voltage by test program. For the parameters without minimum and maximum value in the EC table, the typical value defines the operation range, the accuracy is not guaranteed by spec.

Note 2: The maximum power dissipation decrease if temperature rise, it is decided by TJMAX, θJA, and environment temperature (TA). The maximum power dissipation is the lower one between PDMAX = (TJMAX - TA)/ θJA and the number listed in the maximum table.

Electrical Characteristics (Notes 3, 4) (Unless otherwise specified, HV=50V and TA =25 ℃)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Section (HV)						
HV_OP	HV operation range		20		500	V
HV_ON	HV supply on voltage		7.5	8.5	10	V
HV_OFF	HV supply off voltage		4.5	5.6	6.7	V
IOP	Quiescent current in operation mode	Iout1/2/3/4/5=15mA	100	250	600	μA
IOP_SLEEP	Quiescent current in sleep mode		45	65	95	μA
BVDSS	Breakdown voltage		500			V
Power MOSFET(OUT1/2/3/4/5)						
IOUT	Maximum current range（Note 5）	PWM=100%	5		90	mA
IOUT_MIN	Minimum dimming percentage			1		%
VOUT	Inflection point voltage for constant current	Iout=30mA			6	V
BVDSS	Breakdown voltage		500			V
I²C Interface Section						
VSUP	I²C interface supply voltage		3	3.3	3.6	V
R_SDA	SDA internal pullup resistor		12	15	18	kΩ
R_SCL	SCL internal pullup resistor		12	15	18	kΩ
VH_SDA	SDA high logic level		1.8		5	V
VL_SDA	SDA low logic level		0		1.6	V
VH_ SCL	SCL high logic level		1.8		5	V
VL_SCL	SCL low logic level		0		1.6	V
F_SDA	SDA input frequency			200	300	kHz
F_SCL	SCL input frequency			200	300	kHz
T_LOW	SCL low logic level time		1.5			μS
T_HIGH	SCL high logic level time		1.5			μS
T_N	Noise elimination time			100		nS
T_AA	SCL time between falling edge and effective output				100	nS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_HD.STA	Start hold time		250			nS
T_SU.STA	Start setup time		250			nS
T_HD.DAT	Data hold time		250			nS
T_SU.DAT	Data setup time		250			nS
TR	Input rising time				150	nS
TF	Input falling time				150	nS
TSU.STO	Stop setup time		250			nS
Thermal Regulation Section						
T_{REG}	Thermal Regulation Temperature	Junction temperature		145		°C

Note 3: production testing of the chip is performed at 25°C.

Note 4: the maximum and minimum parameters specified are guaranteed by test, the typical value are guaranteed by design, characterization and statistical analysis.

Note 5: the maximum output current is tested under VD=15V (VD refers to the drain voltage of MOSFET)

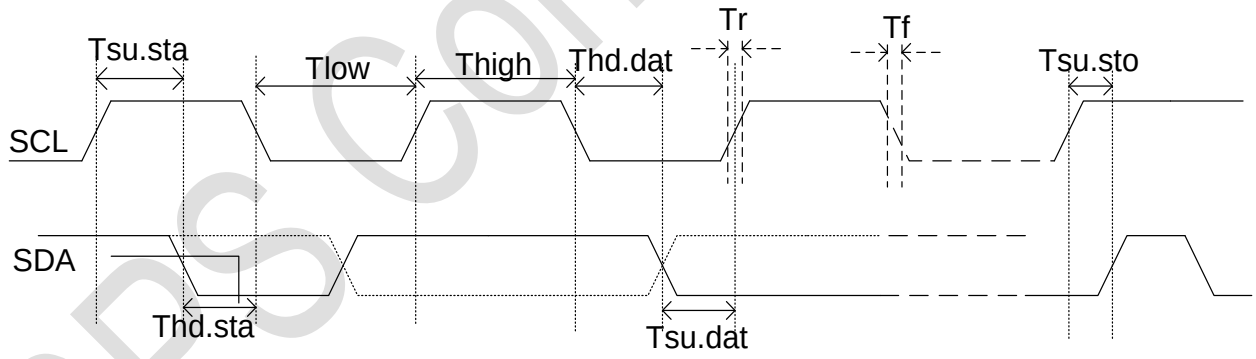


Figure 3: SCL and SDA input waveform

Internal Block Diagram

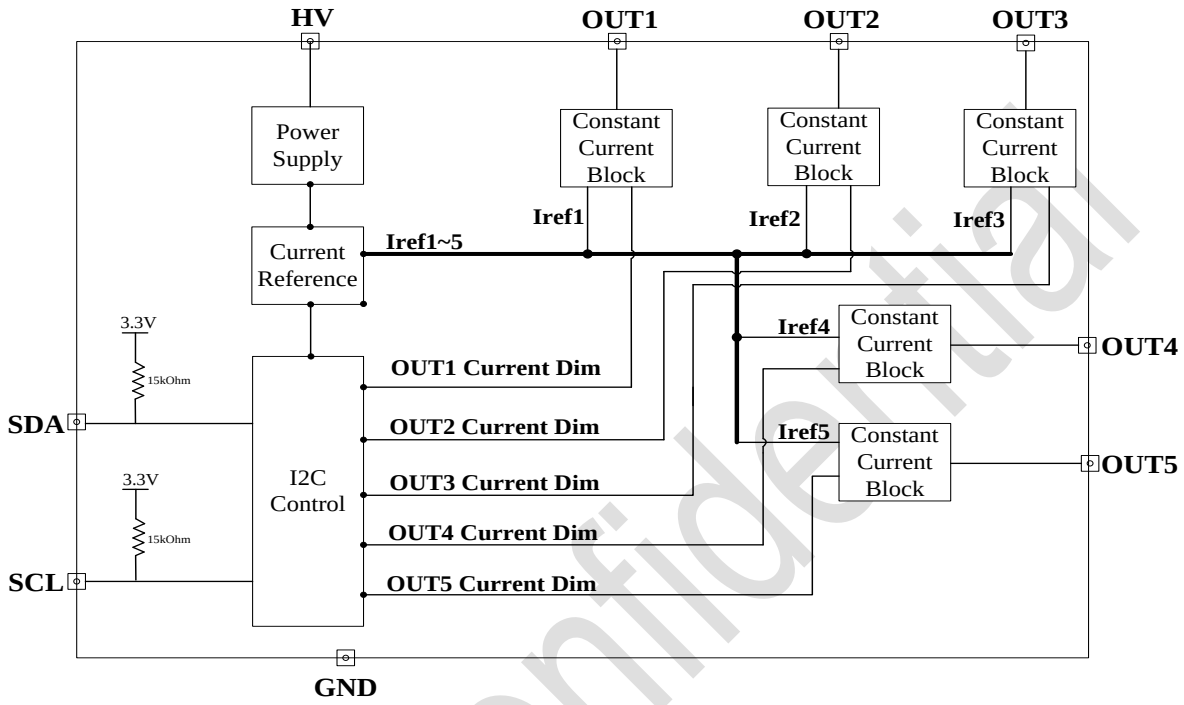


Figure 4: Internal Block Diagram

Application Information

The BP5758D is a five-channel high-precision dimmable constant-current linear LED driver which is targeted for tunable warm/cold/color smart lighting application.

1. Start Up

The IC has 1mA pull-down current during start-up process. When the HV voltage is higher than 8V, the supply module of SDA and SCK starts to work. When the HV voltage is higher than 9.8V, the IC starts to work and wait for the signal of SDA and SCL. If there' s no signal of SDA and SCL, the IC enters sleep mode and the quiescent current is about 85μA. If the signal of SDA and SCL is effective, the IC quits from sleep mode and achieves smart dimming via I²C protocol.

2. The Description of I²C Protocol

The IC integrates I²C protocol module and it is a two-line communication protocol. It has two control signals: clock signal SCL and data signal SDA. The SCL and SDA pins of BP5857D integrate 15kΩ pull-up resistors. The user can configurate the two signals to achieve smarting dimming control. The protocol contains start, stop, data transmission and

acknowledgment control. The detailed protocol is as following:

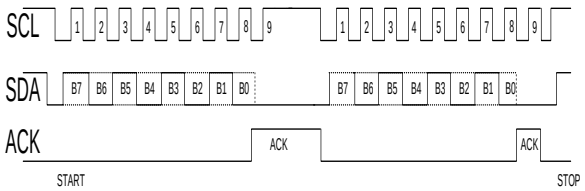


Figure 5: SCL, SDA input signal

2.1 Start and Stop Status Control

The IC are in idle status when data signal (SDA) and clock signal (SCL) at high logic level. When SCL is at high logic level and SDA is at falling edge (logic level: high→low), it is the START condition. Otherwise, when SCL is at high logic level and SDA is at rising edge (logic level: low→high), it is the STOP condition. As shown in figure 6, 9 periods (8Bit+1ACK) of SCL compose one Byte transmission. If addressing is not processed, total 17 bytes can be input. The minimum time for Tsu.sta, Thd.sta, Tsu.sto, Thd.sto is 250ns.

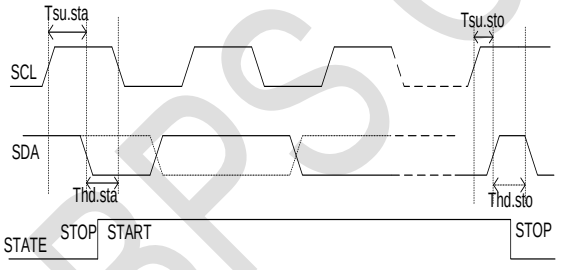


Figure 6: START, STOP status

2.2 Data Transmission Control

I²C is a serial bit transmission protocol and it transfers one bit by every clock pulse. When SCL is at high logic level, SDA must keep stable. When SCL is at low logic level, SDA could change status. When SCL is at the rising edge, the data is written into register. The IC generates the acknowledgement signal ACK at the 9th clock after 8 bits transmission. The ACK signal will pull down the SDA pin. In other words, the IC internally generates an extra response signal after every byte transmission. As shown in figure 7, In order to avoid signal disturbance, Data_IN is only effective when IC is reading SDA signal. The signal must be latched by register and the latching control signal is DATA_LATCH. Tsam.dat is the sampling anti-noise time, which is about 200ns. Tlat.dat is the latching anti-noise time, which is about 200ns. Tsu.dat and Thd.dat must be larger than 250ns. Both Tlow and Thigh higher than 1.5μs is recommended.

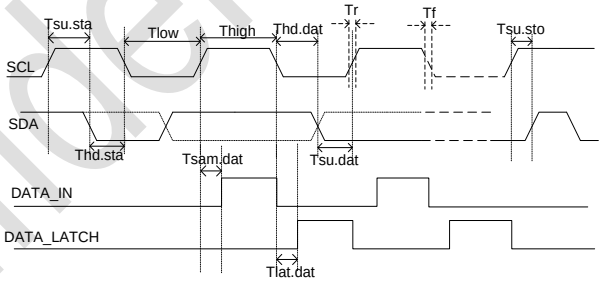


Figure 7: Transmission control diagram

Every 8 bits compose one Byte during transmission. The following table shows the control signal for every bit. All the effective information is executed by the top 17 bytes. The 18th (Byte17) is the setup information for skipping to Byte1. The bytes after Byte17 are the repeating setup of Byte1-Byte16. In conclusion, the effective bytes are 17 bytes before STOP action.

Byte sequence	Operation content
Byte0	Identification bit+sleep mode+addressing for next byte
Byte1	OUT1-OUT5 output current enable setup
Byte2	OUT1 current range (maximum output current) setup

Byte3	OUT2 current range setup
Byte4	OUT3 current range setup
Byte5	OUT4 current range setup
Byte6	OUT5 current range setup
Byte7-8	OUT1 current gray-level setup
Byte9-10	OUT2 current gray-level setup
Byte11-12	OUT3 current gray-level setup
Byte13-14	OUT4 current gray-level setup
Byte15-16	OUT5 current gray-level setup
Byte17	Skip to Byte1：output current enable setup
Byte18	OUT1 current range setup
Byte19	OUT2 current range setup

1.Byte0 (addressing byte) description

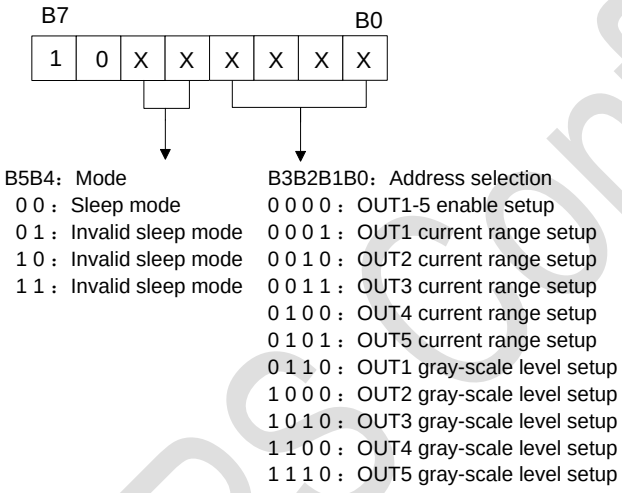


Figure 8: Byte0 setup information

Byte0 is mainly the mode setting and addressing of the chip. B[7:6] = 10 are the identification bits of byte0. B[5:4] are the mode control bits . The IC enters sleep mode when B[5:4]=00. Byte1~Byte16 are forbidden to write in sleep mode, so it is necessary to turn off OUT1~OUT5 before setting the sleep mode. B[4:0] is the addressing byte. The detailed instruction is shown in figure 8.

2.Byte1 (output enable byte) description

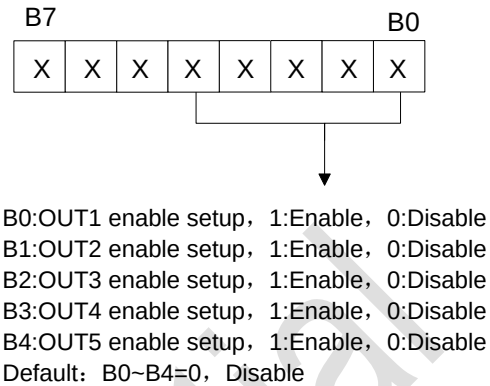


Figure 9: Byte1 setup information

Byte1 is the enable byte of the OUT1-OUT5 channels. B[7:5] is invalid bit which can be any input. The description of B[4:0] is given in figure 9.

3.Byte2 (output current range setup) description

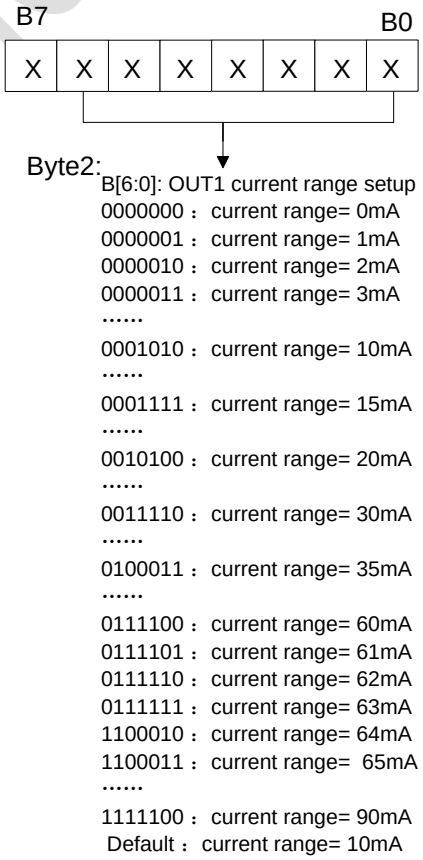


Figure 10: Byte2 setup information

Byte2 is the setting byte of OUT1 current range (maximum output current) and the setup rules are presented in figure 10. If B[5]~B[0] =1, it represents 32mA, 16mA, 8mA, 4mA, 2mA and 1mA respectively. If B[6]=1, it refers to 30mA(not 64mA). The setting of B[7] will not affect the setting of current range. The default current range of out1 is 10mA.

4.Byte3-Byte6 (OUT2~OUT5 output current range setup bytes) description

Byte3-Byte6 are the setting bytes of current range (maximum output current) of OUT2-OUT5 correspondingly. Same as the description of Byte2 in figure 10, the default current range of OUT2- OUT5 is 10mA.

5.Byte7-8 (OUT1 current grey-scale level setup byte) description

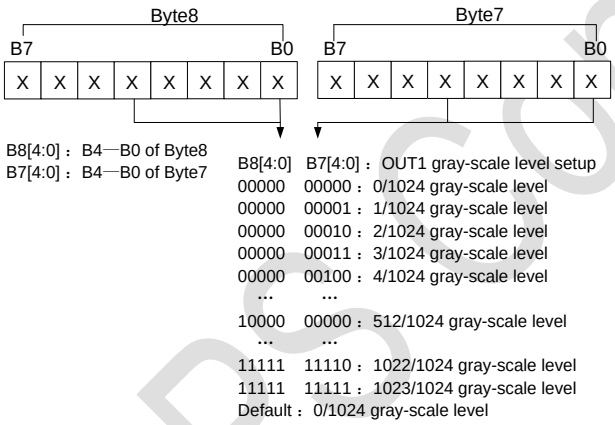


Figure 11: Byte7-Byte8 setup information

In figure 11, the detailed setup information of Byte7-Byte8 is presented. Byte7-byte8 set gray-scale level of OUT1. The grayscale of OUT1 can be adjusted by 1024 levels. B[4:0] of Byte8 and B[4:0] of Byte7 determine the output grayscale of OUT1 together. Shown in figure 11, the default output grayscale is zero.

6.Byte9-16 (OUT2~5 current grey-scale level setup byte) description

Byte9-10 are the current grey-scale level setup byte of OUT2. Byte11-12 are the current grey-scale level setup byte of OUT3. Byte13-14 are the current grey-scale level setup byte of OUT4. Byte15-16 are the current grey-scale level setup byte of OUT5. Their gray-scale level setting method is as same as OUT1 in figure 11.

2.3 Application Example

When the chip changes status from normal operation mode to sleep mode, it should be noted that the output of the channel must be turned off before entering sleep mode. The output will be unstable if the channels are not turned off in advance as Byte1~Byte16 are forbidden to write in sleep mode. The example for entering sleep mode is as following:

MCU program:

Start1: 10110000 (write byte0, normal mode, select byte1)

00000000 (write byte1, set OUT1~5 output disable)

Stop1。

Start2：10000000（write byte0， B5B4=00 and enter sleep mode)

Stop2。

Select OUT1-5 to output together. The maximum current of OUT1~3 is 40mA with 2/1024 grayscale of OUT1, 512/1024 grayscale of OUT2 and 1022/1024 grayscale of OUT3. The maximum current of OUT14~5 is 60mA with 512/1024 grayscale of OUT4 and 1022/1024 grayscale of OUT5:

Start：10110000（write byte0，normal operation mode，select byte1）

00011111（write byte1，set OUT1~5 output enable）

00101000 （write byte2，set OUT1 current range: 40mA）

00101000 （write byte3，set OUT2 current range: 40mA）

00101000 （write byte4，set OUT3 current range: 40mA）

00111100 （write byte5，set OUT4 current range: 60mA）

00111100 （write byte6，set OUT5 current range: 60mA）

10100010（write byte7）

10100000（write byte8，byte7 and byte8 set the grayscale 2/1024 of OUT1 together）

10100000（write byte9）

10110000（write byte10，byte9 and byte10 set the grayscale 512/1024 of OUT2 together）

10111110（write byte11）

10111111（write byte12，byte11 and byte12 set the grayscale 1022/1024 of OUT3 together）

10100000（write byte13）

10110000（write byte14，byte13 and byte14 set the grayscale 512/1024 of OUT4 together）

10111110（write byte15）

10111111（write byte16，byte15 and byte16 set the grayscale 1022/1024 of OUT5 together）

Stop。

Select OUT4-5 to output together. The maximum current of OUT4~5 is 60mA with 2/1024 grayscale of OUT4, 512/1024 grayscale of OUT5. After 1mS, the grayscale of OUT4 is changed to 512/1024 and the grayscale of OUT5 turns to 2/1024:

Start1：10110000（write byte0，normal operation mode，select byte1）

00011000（write byte1，set OUT1~3 disable and OUT4~5 enable）

00000000（write byte2，set OUT1 current range:0mA）

00000000（write byte3，set OUT2 current range:0mA）

00000000（write byte4，set OUT3 current range:0mA）

00111100 （write byte5，set OUT4 current range:60mA）

00111100 （write byte6，set OUT5 current range:60mA）

Stop1

Start2：10111100（write byte0，normal operation mode，select byte13）

10100010（write byte13）

10100000（write byte14，byte13 and byte14 set the grayscale 2/1024 of OUT4 together）

10100000（write byte15）

10110000（write byte16，byte15 and byte16et the grayscale 512/1024 of OUT5 together）

Stop2

Start3：10111100（write byte0，normal operation mode，select byte13）

10100000（write byte13）

10110000（write byte14，byte13 and byte14 set the grayscale 512/1024 of OUT4 together）

10100010（write byte15）

10100000（write byte16，byte15 and byte16 set the grayscale 2/1024 of OUT5 together）

Stop3

3. Thermal regulation

BP5758D has thermal regulation function to balance the power delivering and temperature increasing. To improve the system reliability, the output current will decrease after the BP5758D temperature reaches over temperature protection point.

4. PCB Layout design

Suggestion for BP5758D PCB layout：

Exposed Pad

BP5758D uses ESOP-8 package to improve the thermal dissipation. Put the ground copper of exposed pad as large as possible for better thermal resistance and power dissipation.

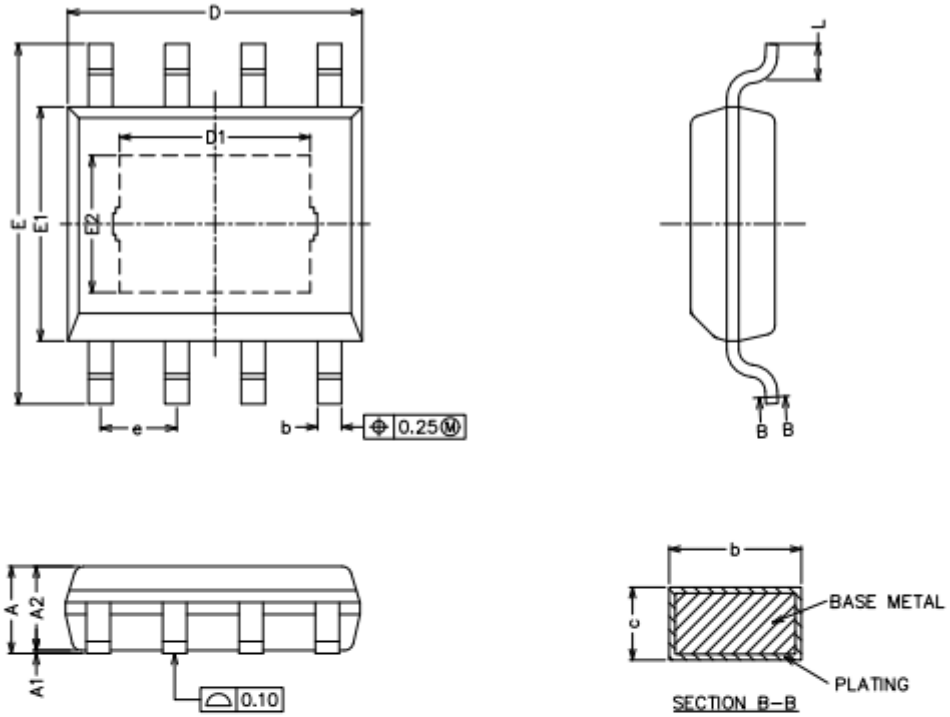
SDA and SCL Signal Wires

The wires from MCU signal output to SDA and SCL pins of BP5758D should be as short as possible. Avoid the interference of other noise to the digital signal on PCB.

HV Pin Routing

Pin2(HV) is the high voltage pin. Keep these high voltage pin and traces as far away as possible from low voltage components and traces (e.g., SDA, SCL, etc.).

Physical Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.35	–	1.75
A1	0.00	–	0.15
A2	1.25	1.40	1.65
b	0.30	–	0.50
c	0.10	–	0.25
D	4.70	4.90	5.10
D1	3.02	–	3.50
E	5.80	–	6.40
E1	3.70	3.90	4.10
E2	2.1	–	2.6
L	0.40	0.60	1.25
e	1.17	1.27	1.37

Revision Information

Revision	Date	Notes
Rev.0.9	2020/11	Preliminary
Rev.0.91	2021/01	1. Add the external pull-up resistors to Vcc at SCL and SDA pins, suggested resistance: 1kΩ~4.3 kΩ 2. Updated the package information
Rev.1.0	2021/5	1. Updated the ectable
Rev.1.1	2021/7	1. The minimum value of SCL and SDA input low level is updated to 0V

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