Technical Note

Termination for Point-to-Point Systems

Introduction

Because digital signal rates in computing systems are increasing at an astonishing rate, signal integrity issues have become far more important to designers. At higher frequencies, PCB traces can no longer be treated as just wires used to connect digital components together— they become radio frequency (RF) transmission lines. Therefore, a basic understanding of transmission line theory is important to ensure signal integrity in today's high-speed digital systems.

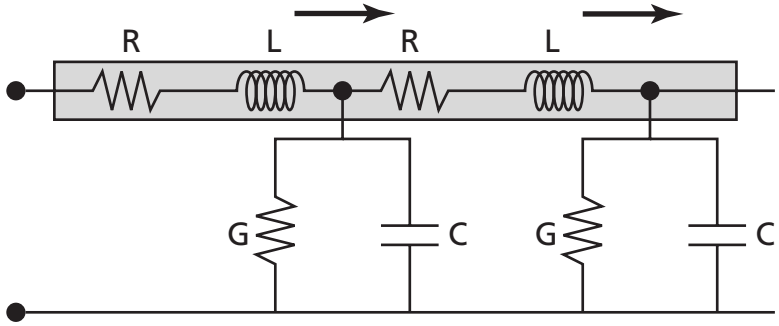
There are two major areas that affect signal integrity. The first is transmission line effects such as ringing and reflections. The second area is the interaction between circuits, such as crosstalk and noise on the power plane. With modeling, these transmission lines and interaction of adjacent signals can be passed with minimal attenuation and distortion. Micron provides both IBIS and Spice models to help in these areas (see ww.micron.com/models).

Transmission Line Theory

Understanding electromagnetic waves and the theories (Maxwell's Equations) that define their behavior is not simple, but understanding their effects in your application can be done without too much trouble.

One of the basic concepts of transmission lines is characteristic impedance (see Figure 1).

Figure 1: Transmission Line



The characteristic impedance of a line is defined as Z_0 (see Figure 2), where R is the resistance per unit length, L is the inductance per unit length, G is the conductance per unit length, and C is the capacitance per unit length. The conductance per unit length is due to loss through dielectric material separating the two traces. You can safely assume G = 0

at speeds below 1 GHz. In some circumstances you can also assume R to be zero, but as the frequencies are increasing, you have to account for the skin effect. If you Assume both G and R are zero, the transmission line would be considered loss less equation 2 (see Figure 3 on page 2).

Figure 2: Equation 1: Z_0 Assuming G = 0

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \sqrt{\frac{R + j\omega L}{j\omega C}}$$

ω - angular frequency = $2\pi f$

j - $\sqrt{-1}$

Figure 3: Equation 2: Z_0 Loss Less Transmission Line

$$Z_0 = \sqrt{\frac{L}{C}}$$

The skin effect is a phenomenon where conductivity decreases as the frequency increases. The signal is carried in a very thin layer of the conductor's surface. The thickness of this layer is dependent on the frequency of the signal, Equation 3 (see Figure 4) causing the resistance (R) of the transmission line to increase with frequency.

Figure 4: Equation 3: Skin Depth for Copper

$$\delta = \frac{2.6}{\sqrt{f}} \text{ in inches} \qquad \delta = \frac{6.6}{\sqrt{f}} \text{ in cm}$$

Figure 5: Equation 4: Skin Depth Resistance

$$R_s = \sqrt{\frac{\pi f \mu}{\sigma}} \qquad R_{a.c.} = \sqrt{\frac{R_s \ell}{w}}$$

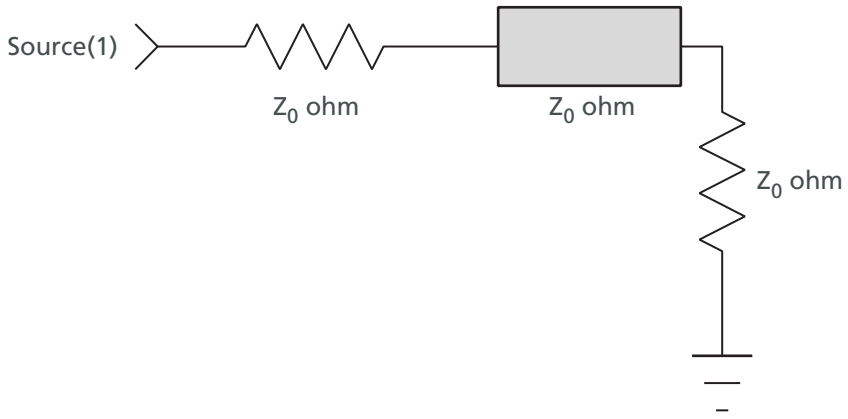
f = frequency
μ = permeability
σ = conductivity

f = frequency
μ = permeability
σ = conductivity
ℓ = length
w = width

At the speed some of the point-to-point DDR systems are running, the skin depth is reaching to a few tenths of a mil (0.0002 inches) for the conducting layer, in turn increasing the AC resistance. The skin effect is the main reason one cannot ignore the resistance in calculating the characteristic impedance of a transmission line.

Characteristic impedance has units of ohms. When a transmission line is terminated at both ends with its characteristic impedance, the line is said to be matched (see Figure 6 on page 3). Being matched means no reflections occur on the line. A matched line is the optimal line for passing high-frequency signals. If a transmission line is not matched (terminating impedances don't match the characteristic impedance) reflections of the signal will occur. Reflections on the line distort the desired signal and if the distortion is large enough, the signal cannot be detected reliably by the receiver.

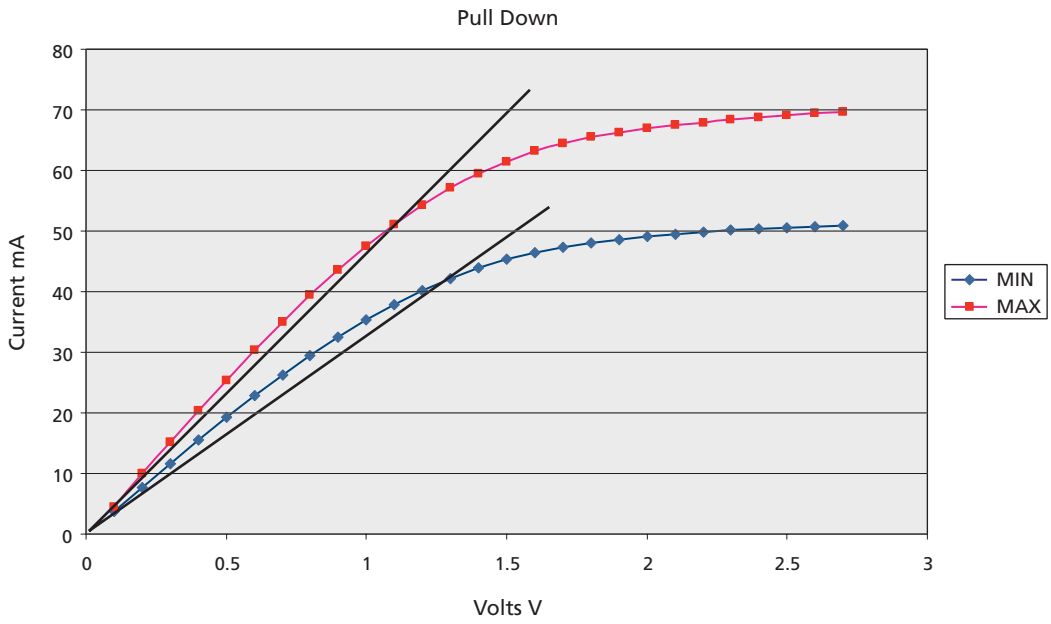
Figure 6: Matched Transmission Line (Source Impedance = 0)



Termination

Termination is used to match the driver impedance to the transmission line impedance when mismatch case exists. Where output driver impedance + termination impedance = Z_0 of the line. If the characteristic output drive impedance is not known, it can easily be approximated with the dV/dI curves. These curves can be found in the IBIS model for the device driver. To extract the driver impedance from the curves, divide the delta V by delta I in the operating range of the output driver (see Figure 7). From this figure, take the delta on the two linear lines drawn from 0 to about 1.5V.

Figure 7: Standard Pull-Down (Operating Range 0–1.5V)

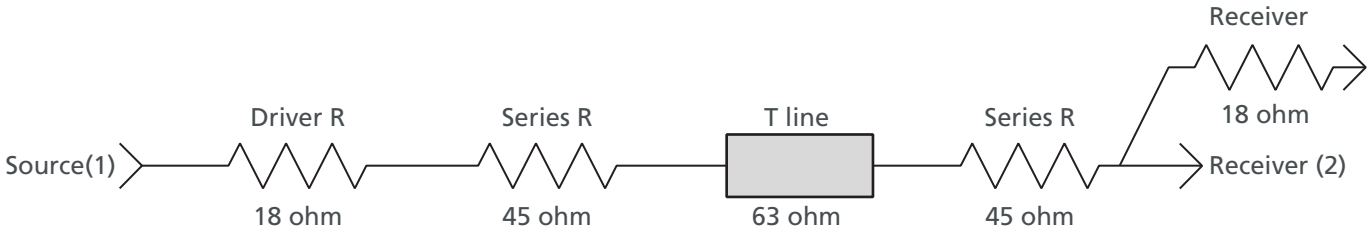


As the drive strength of a driver is increased, its impedance goes down. However, there are limits to the range of impedances that can be easily obtained for a driver. The characteristic impedance of microstrip is also limited to a range because of physical dimensions. The characteristic microstrip impedance is a function of the dielectric constant of the substrate, the thickness of the substrate, and the width of the trace and frequency of the signal. As its width increases the characteristic impedance drops. For 4.5 mil FR4 substrate and a 5 mil line, the characteristic impedance is ≈ 63 ohms.

If, because of layout concerns, the widest the microstrip line can be is 5 mils, the driver impedance would have to be 63 ohms. If the microstrip lines can be increased to 10 mils (characteristic impedance of ≈44 ohms) the driver impedance could be lowered to 44 ohms. In some manner, driver impedance should be matched to the characteristic impedance of the transmission line. If the driver impedance cannot be increased to the optimum impedance, a series resistor can be placed next to the driver to raise the impedance to the desired level (see Figure 8 on page 4). For example, if the drive impedance is ≈18 ohms, the series resistor would need to be 45 ohms for a 63 ohm transmission line. If the line needs to be driven from both ends (DQ line), two series resistors would be needed (see Figure 9 on page 5).

Figure 8: Series Resistor

Figure 9: Two-Series Resistor



As previously indicated, a fully matched transmission line is the optimum interconnection between devices. However, a fully matched line also divides the signal in half (half the signal in the driver impedance and half in the load). So the question arises: Is there another way to connect the devices without reducing the signal by half? The answer is, "Yes."

If only one end of a transmission line is matched, signals will reflect off the unmatched end and then terminate into the matched end. The configuration in which the driving impedance is matched and the receiving end is not is known as back terminating (see Figure 10 on page 5). Signals that come from the source travel down the transmission line, reflect off the unterminated end, then travel back through the transmission line and terminate in the source resistor. Although there is a reflection, this reflection does not distort the signal at the receiving end.

Figure 10: Back Terminating

For point-to-point DQ connections there are two main issues: the system impedance, and the load capacitance. With a particular capacitance and drive impedance there is an ultimate limit on the maximum data rate that can be attained in a digital system. As the capacitance or drive impedance goes up, maximum data rate goes down. Likewise, as the capacitance or drive impedance goes down, the maximum data rate goes up. This is why it is so important to reduce the input capacitance on digital receivers.

The issue of reducing the drive impedance is not quite so simple. Reducing the drive impedance without reducing the impedance of the connecting transmission line will create signal integrity problems. The optimal solution for point-to-point DQ connections would be to match the driver impedance to the characteristic impedance of the transmission line, and for this impedance to be as low as possible. This would allow a direct connection with the highest possible speed and with no additional components.

One problem a driver has is that its impedance is not constant. As the levels change from LOW to HIGH or HIGH to LOW, the impedance varies. The driver also has some parasitic capacitance and inductance that makes the drive impedance not purely resistive. A series resistor can reduce the effect of drive impedance variation on signal integrity degradation.

If the above guidelines are taken into account, point-to-point connections are simple to make but they must be analyzed with the known parasitics. Sometimes it may be beneficial to mismatch the line with a smaller drive impedance. A smaller drive impedance can sometimes provide a higher data rate with little sacrifice in signal integrity.

When multiple drops are required (clocks and addresses), the configuration analysis is no longer simple and a more complicated analysis is required. Various parameters needed to be changed and balanced to get optimal performance.

Point-to-Point Example: DQ Topology

This topology was selected by considering a combination of eye pattern, component count, and power consumption. The topology selected for this DQ, point-to-point connection uses a series resistor located midway between the driver and receiver, and supports both READs and WRITEs between the components. From the above discussion, this is not an optimal configuration. A compromise was made to support the use of only one resistor.

Note: All DQ point-to-point connection analysis is done assuming a 400 MB/sec data rate on 4.5 mil FR4 with SSTL2 driver receiver.

Figure 11: Example Simulation Net Assuming 2-Inch Traces

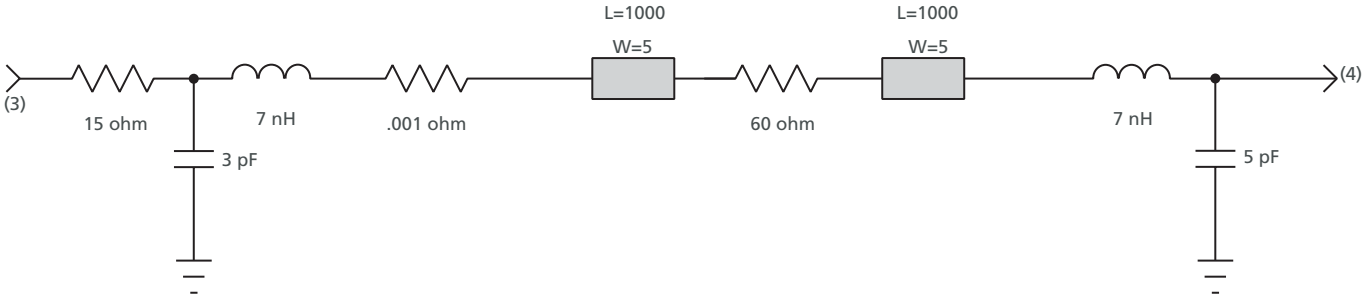
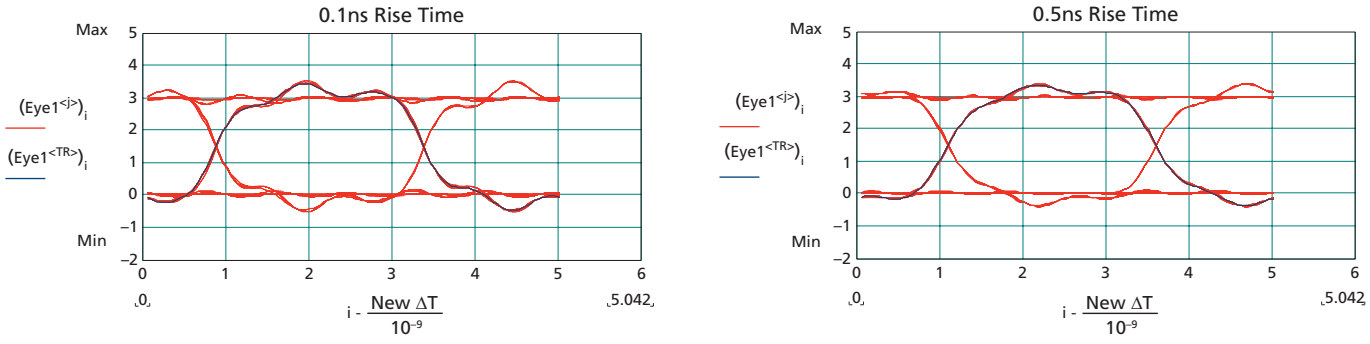


Figure 12: Example Topology Results – Linear Simulation, Driver Impedance = 15 Ohms)



Note that the resistance used in these examples is 60 ohms. A 60 ohm resistor was used as a compromise between using a single resistor, and rise time and overshoot. For this topology, a lower resistor could be selected if more overshoot can be tolerated. See the section on resistor sizes.

Resistor Value Variations

The effect of resistor value on the example net (linear simulation, driver impedance 15 ohms) are shown in Figure 13 through Figure 16. These graphs demonstrate the effects of mismatching the characteristic impedance. Note that mismatching the drive impedance to the transmission line affects signal integrity. Also note that the 45 ohm case has better transitions than the selected topology but with a little more overshoot.

Figure 13: Resistor Value – 30 Ohms

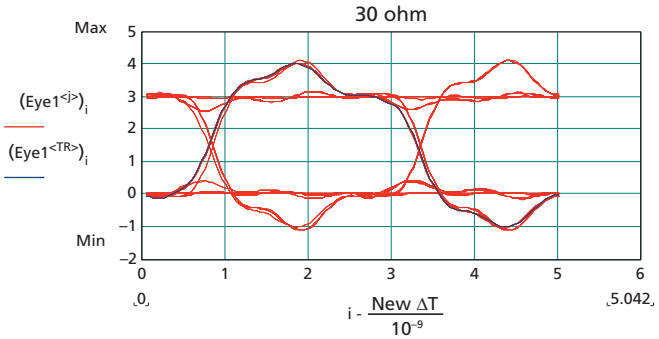


Figure 14: Resistor Value – 45 Ohms

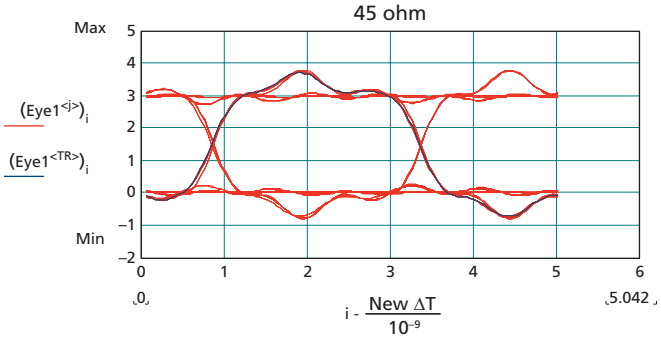


Figure 15: Resistor Value – 75 Ohms

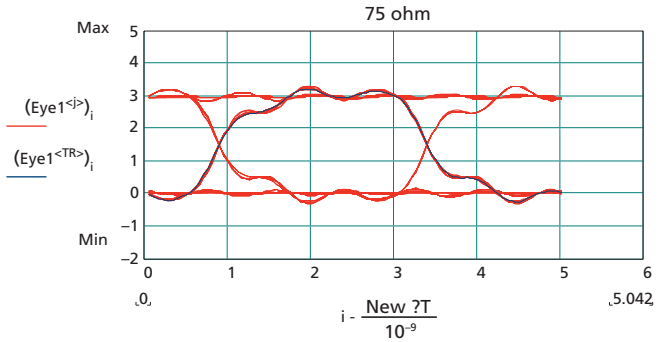
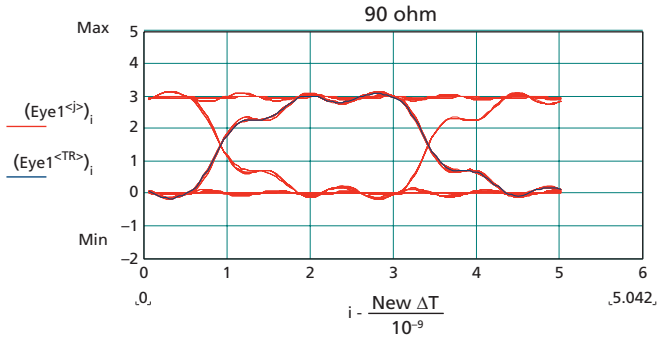


Figure 16: Resistor Value – 90 Ohms



Rise Time in Mismatched Simulations

The rise time can also play a large role in signal integrity. The graphs in Figure 17 through Figure 20 demonstrate the affects of reducing the rise time to improve signal integrity. It is always a good idea to use the slowest rise times that will meet the required timing budget.

Figure 17: Characteristic Impedance Mismatch Simulation – 0.1ns Rise Time

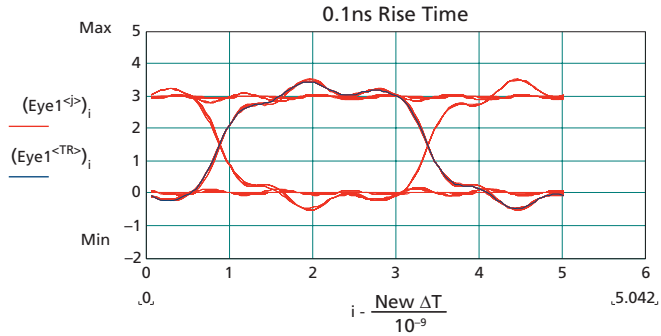


Figure 18: Characteristic Impedance Mismatch Simulation – 0.25ns Rise Time

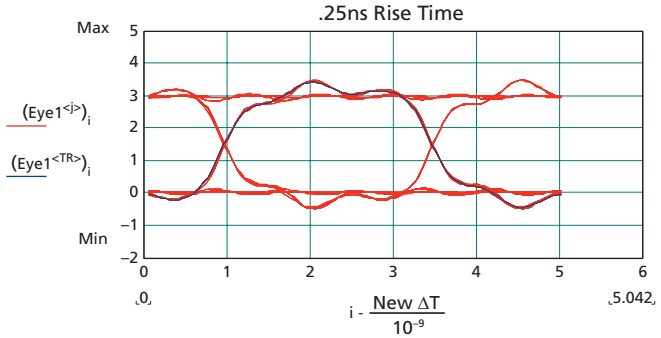


Figure 19: Characteristic Impedance Mismatch Simulation – 0.5ns Rise Time

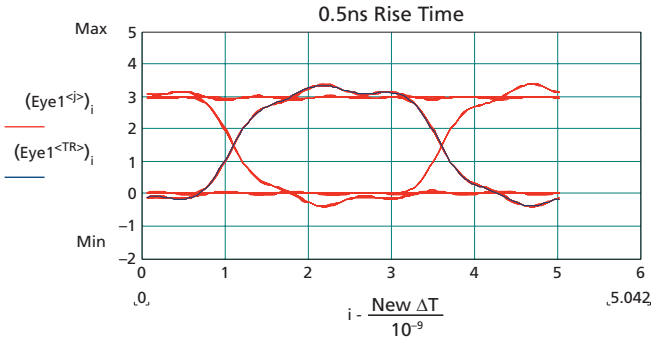
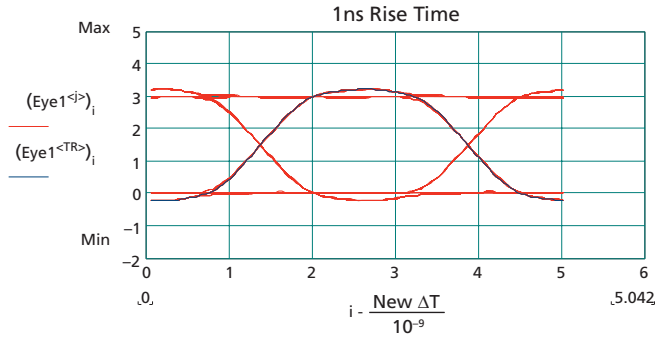


Figure 20: Characteristic Impedance Mismatch Simulation – 1ns Rise Time



Conclusion

The question is a common one—what does Micron recommend for termination? Ultimately, the best solution is to simulate your design to ensure clean signals and good data eyes.

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Revision History

Rev. B 3/11

- Updated formats and styles

Rev. A 6/01

- Initial release