IR11688 SmartRectifier™ Control IC Design Notes

Authors: Helen Ding
Peter Green

Application Note

About this document

Scope and purpose

The purpose of this document is to provide a comprehensive functional description and guide to using the IR11688 dual channel synchronous rectification control IC in the output of a LLC switch mode power supply (SMPS). The scope applies to all technical aspects that should be considered in the design process, including calculation of external component values, MOSFET selection, PCB layout optimization as well as additional circuitry that may be added if needed in certain cases.

Intended audience

Power supply design engineers, applications engineers, students.

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1 Introduction and device overview

The IR11688 synchronous rectifier (SR) control IC drives a pair of N-channel power MOSFETs forming the rectifying output stage of a resonant half-bridge converter. The drain to source voltage of each SR MOSFET is directly sensed to determine the level of conducted current so that the MOSFET can be turned on and off in close proximity to the zero current transition. Built in shoot-through protection logic prevents both channels from being able to ever turn on at the same time. Internal blanking, reverse current protection and double-pulse suppression allow reliable operation in all operating modes.

The IR11688 precisely controls switching on and off of the synchronous MOSFETs thereby bypassing their body diodes during the secondary conduction phases and emulating the rectifying action of a dual diode rectifier while eliminating the majority of conduction losses. The MOSFET drain to source voltages are sensed at millivolt levels to determine the magnitude and polarity of the drain current so that the IR11688 can switch the gates on and off appropriately. The high voltage input structure allows the IR11688 to withstand up to 200 V from direct connection to each drain pin.

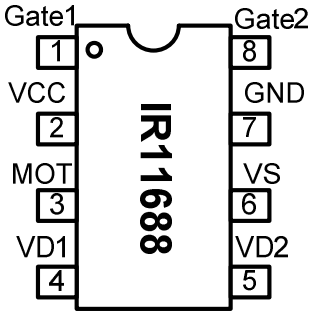
The IR11688 based smart synchronous rectifier offers significant efficiency improvement in resonant converters over the full load range. Replacement of a Schottky diode output rectifier with the IR11688 combined with a pair of correctly selected high performance MOSFETs, provides significantly lower power dissipation and efficiency improvement. PCB space savings due to the IR11688's small SO-8 package are further aided by reduced MOSFET heat dissipation.

The IR11688 can operate from a wide Vcc supply voltage ranging from 4.75 V to 20 V enabling it to be supplied from the output in a 5 V system and eliminating the need for an auxiliary transformer winding. A logic level MOSFET is required for low output (low Vcc) voltage applications.

A built in arming and triggering mechanism allows correct switching on and off of the SR MOSFET under all system conditions, making it superior to a basic self-driven SR scheme or earlier generations of SR controller.

In addition the IR11688 enters a power saving mode if both VD sensing inputs do not switch for more than a waiting time (typically 500 µs). Supply current reduces to a few hundreds of micro-Amps, greatly reducing quiescent power loss in standby mode and improving system standby and light load efficiency.

IR11688 is available in a SO-8 package. The pin out is shown below:



PIN#	Symbol	Description
1	GATE1	Gate Drive Output 1
2	VCC	Supply Voltage
3	MOT	Minimum On Time Program Input
4	VD1	SR MOSFET 1 Drain Voltage Sense
5	VD2	SR MOSFET 2 Drain Voltage Sense
6	VS	SR MOSFET Source Voltage Sense
7	GND	Analog and Power Ground
8	GATE2	Gate Drive Output 2

Figure 1 IR11688 Dual SmartRectifier™ control IC pin assignment

2 SmartRectifier™ concept and IR11688 operation

The SmartRectifier™ control technique is based on sensing the voltage across the MOSFET drain to source and comparing it with two internal negative thresholds determine the correct points of gate turn on and off. The first negative threshold V_{TH2} detects current through the body diode determining when to turn on. A second negative threshold V_{TH1}, which is in the range of milli-Volts, determines the level at which the gate is turned off.

A typical schematic of an LLC resonant half-bridge converter using an IR11688 to drive two SR MOSFETs is shown in figure 2:

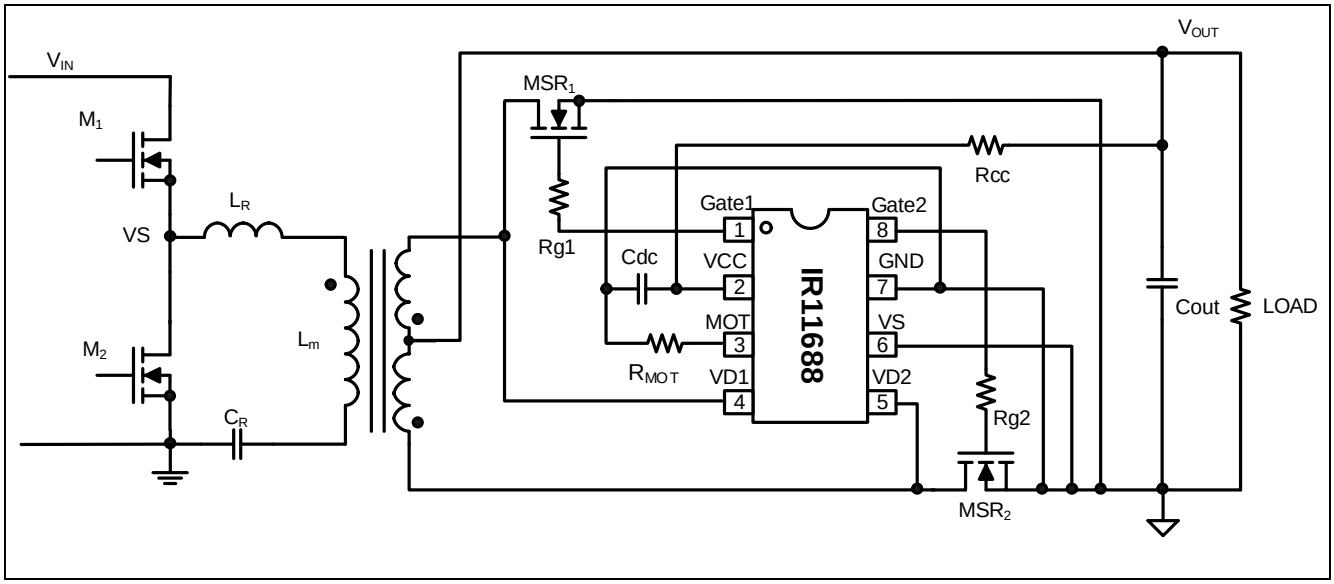


Figure 2 Typical schematic of a resonant half-bridge converter with IR11688

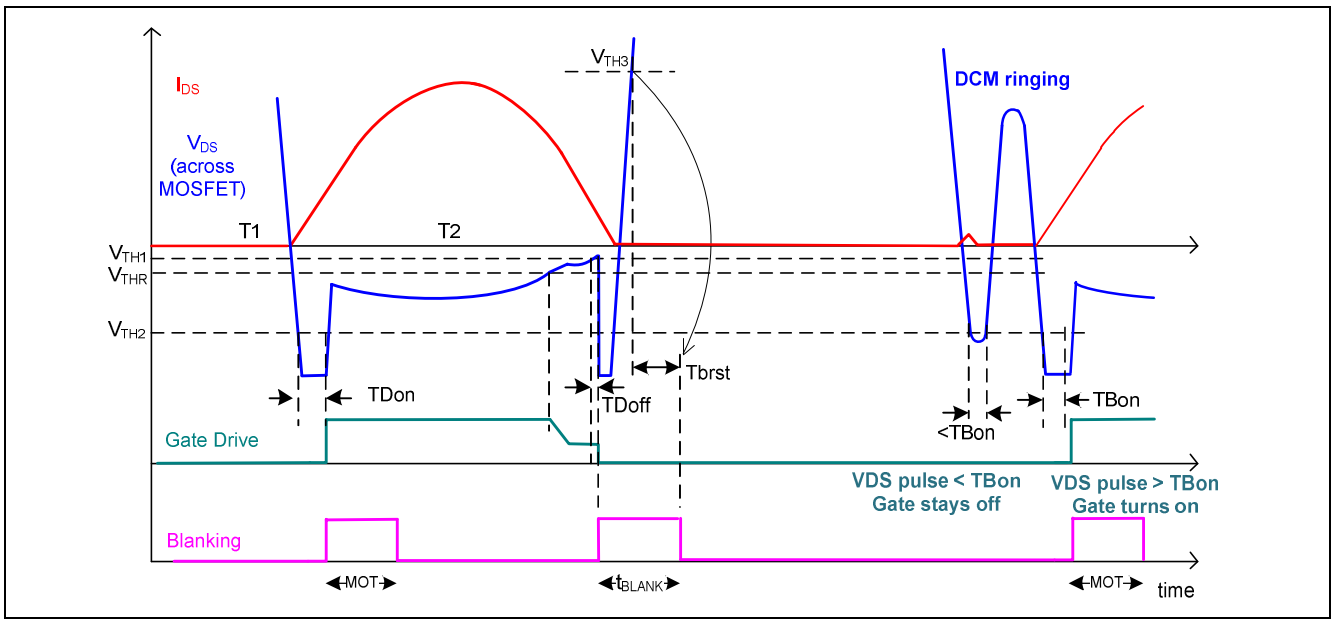


Figure 3 Typical operating waveform of IR11688

The operating waveforms shown in figure 3 show one side of the split secondary dual MOSFET synchronous rectifier. During period T1 there is no current in this branch of the secondary. The T2 phase begins when the corresponding primary switch is turned on and energy is transferred through the transformer to be

delivered to load through the output rectifier circuit. At this point the conduction phase of the branch SR MOSFET is initiated and current starts flowing through its body diode, producing a negative V_{DS} voltage. The body diode has a much higher voltage drop than the turn-on threshold V_{TH2} causing the IR11688 to drive the gate of the SR MOSFET on to bypass it.

When the MOSFET is turned on the instantaneous sensed voltage reduces to $R_{DSon} \cdot I_D$. This voltage level being much lower than body diode forward voltage drop is sensitive to parasitic ringing generated by the transformer leakage inductance and MOSFET output capacitance. To avoid mis-triggering and resulting premature gate turn-off, a blanking period (MOT) is set that disables V_{TH1} triggering for a minimum period of time set by an external resistor. This avoids false triggering of the turn-off immediately after turning-on, by maintaining the MOSFET on for a minimum amount of time.

Once the SR MOSFET has been turned on, it will remain on until the rectified current decays to a level where V_{DS} reaches the regulation threshold V_{THR}. At this point the gate drive pull up is switched off and the gate drive output remains in a high impedance state with a weak pull down to slowly discharge the gate voltage. The MOSFET channel resistance increases as gate voltage drops moving towards the linear region of operation and thereby maintaining the negative V_{DS} voltage drop lower than the turn off threshold V_{TH1}. The discharge circuit is maintained to keep V_{DS} voltage regulated around V_{THR} as current falls, thereby extending the MOSFET conduction period.

Eventually as the MOSFET channel current reduces further towards zero, the V_{DS} voltage crosses threshold V_{TH1} and the IR11688 turns the gate off. The gate drive regulation function is illustrated in figure 4:

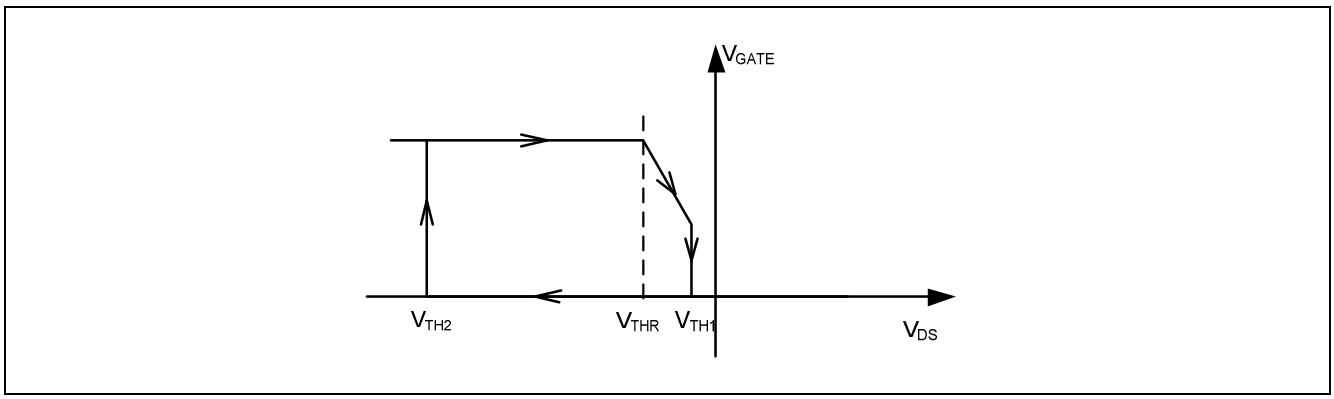


Figure 4 IR11688 voltage sensing thresholds

When the IR11688 turns the gate off current will again start flowing through the body diode, which causes the V_{DS} voltage to make a sharp negative transition. Depending on the amount of residual current, V_{DS} may once again exceed the turn on threshold V_{TH2}. For this reason re-triggering is disabled after the gate drive has been switched off until the controller has re-armed.

The re-arming sequence requires V_{DS} to cross the V_{TH3} threshold and remain above it for a period denoted as t_{BRST}. If this does not occur the gate drive will remain low for a period of t_{BLANK}, after which time re-arming will occur automatically.

To achieve high system efficiency combined with low standby loss, the IR11688 incorporates a programmable minimum on time (MOT). This feature offers flexibility when using the IR11688 in various applications operating at different switching frequencies. The MOT function effectively sets the shut-down point at light load. During normal operation, the designer sets the minimum on time to be shorter than the secondary conduction period. At progressively lighter loads, the conduction period reduces until it is eventually shorter than the MOT. If the IR11688 detects no voltage drop signifying no SR drain current the MOT protection function causes the gate drive to be disabled for the next cycle. This MOT protection operates whether or not the SR gate drive is on, that is if conduction is through drain-source channel or the

body diode. In this way the IR11688 does not drive the gate at light loads and therefore consumes minimal power improving system efficiency.

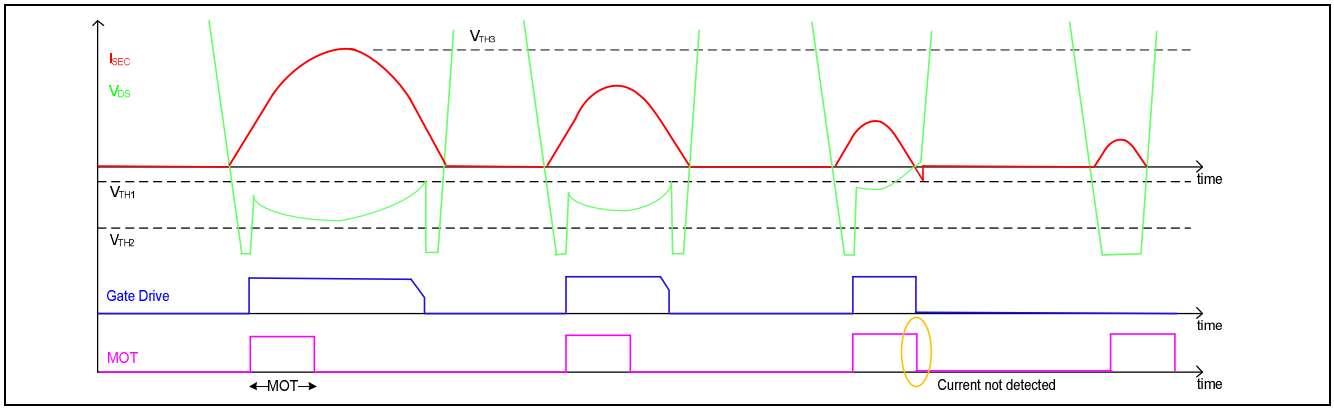


Figure 5 MOT protection as load decreases

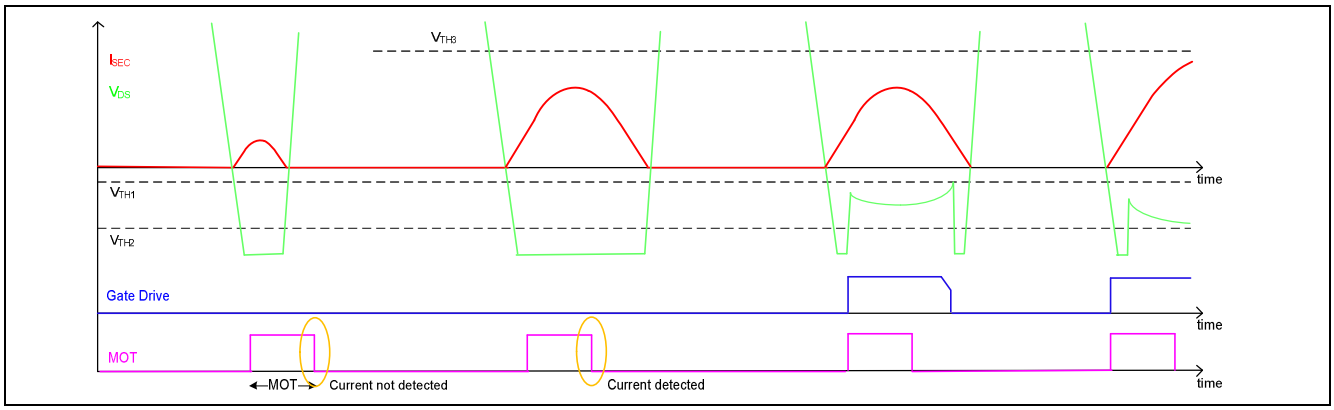


Figure 6 Gate drive resuming as load increases

The IR11688 includes a turn-on leading edge blanking function to prevent misfiring that could be triggered by high frequency ringing in DCM operation. In DCM mode the drain voltage of the SR MOSFET can resonate when secondary current transitions in each half cycle. This V_{DS} ringing as shown in figure 3 could drop below zero volts under certain conditions, such as higher body diode voltage drop or longer body diode reverse recovery. To avoid false triggering by negative ringing, the IR11688 only triggers if V_{DS} is lower than V_{TH2} longer than blanking time T_{bon}. Therefore, in the case of a short spike or ringing the IR11688 will not switch on the MOSFET gate and the internal MOT timer will not be initiated preventing a false trigger event and resulting shoot through current. In a regular conduction cycle V_{DS} remains lower than V_{TH2} for more than T_{bon}, and so the gate turns on after T_{bon} expires.

The total turn on delay T_{don} is the sum of T_{bon} blanking time and the propagation delay of internal comparator. The turn-on delay T_{don} and the MOT time limit the minimum conduction time of the secondary rectifiers and hence, the maximum switching frequency of the converter with which it can effectively operate.

3 Design and selection of passive components

3.1 IR11688 V_{CC} supply

The IR11688 may be biased from the output voltage if Vout falls within the range of 4.75 V to 20 V. A small RC filter is recommended between Vout and Vcc for noise filtering. A decoupling capacitor of at least 1 uF is necessary to prevent noise from interfering with the correct operation of the IR11688, with resistor value in 5~10 Ω. Although the IR11688 accepts up to 20 V supply voltage, it is suggested in higher output voltage systems to limit the supply voltage to 12 V~15 V where standard SR MOSFETs are used. This reduces gate drive switching losses since the gate drive outputs are not internally clamped. The Vcc clamping circuit could be a simple shunt zener diode with a current limit resistor; however the following simple series voltage regulator circuit is more efficient.

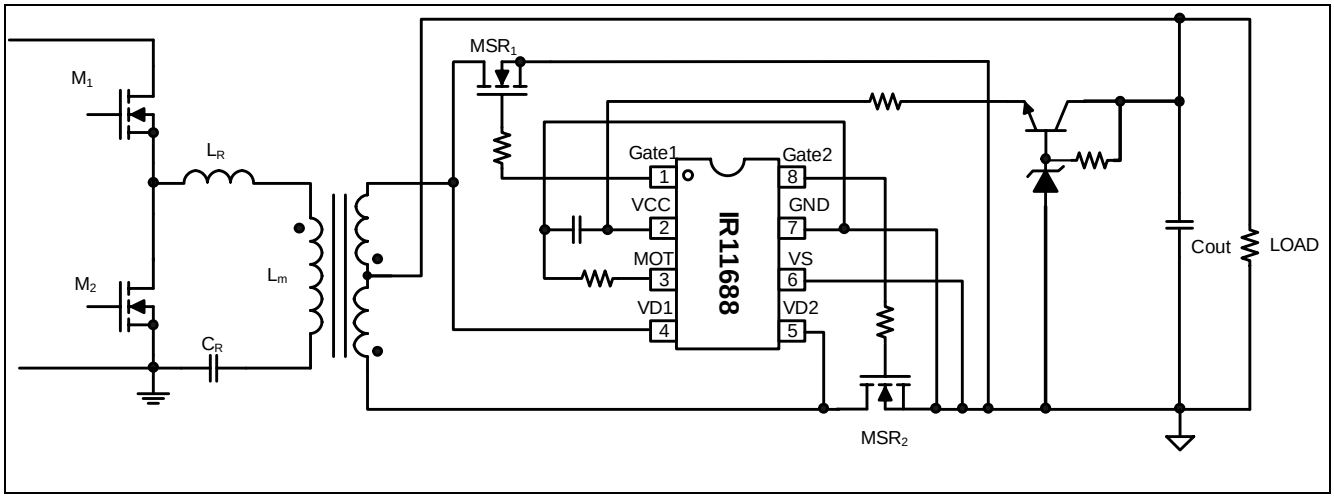


Figure 7 IR11688 Vcc clamping circuit

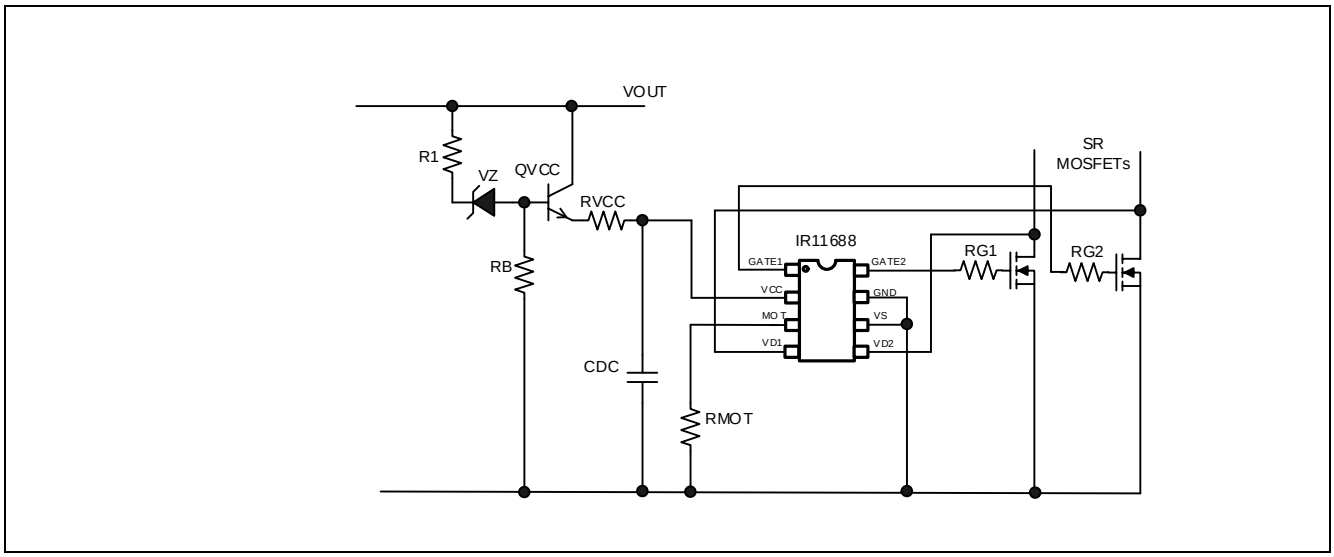


Figure 8 Simple VCC level shift supply circuit

Figure 8 shows an alternative supply circuit for V_{CC} based on a voltage level shift. Vcc is determined by V_{out} minus the value of $V_Z + V_{BE}$ with typically 0.5 V drop on R1. On startup as Vout rises it must exceed $V_Z + V_{BE}$ +

0.5 + V_{CCON} before the IR11688 gate drives are enabled (the voltage drop through R_{VCC} is negligible since R_{VCC}≤10 Ω). This prevents possible shoot through from occurring due to the gates potentially being switched on due to ringing oscillations during start up.

3.2 MOT resistor calculation

The MOT is linear in relation to the resistor value R_{MOT}, the following formula can be used to determine the required value:

$$R_{MOT} = 5 \cdot 10^{10} t_{MOT} \quad (1)$$

The value of R_{MOT} should not be lower than the minimum recommended on the datasheet.

3.3 Gate driver resistor

Since IR11688 based synchronous rectification turns the SR MOSFETs on and off at V_{DS} levels close to zero, the gate resistors do not have an impact on the transitions and can be designed in order for the gate loop to be optimized and oscillations should be minimized as much as possible in regular operations. Therefore, assuming the total gate trace loop inductance (L_g) is known, (a first order estimation can be 1 nH/mm of physical trace length), the minimum recommended gate resistor will be:

$$R_{g_{loop}} > 2\sqrt{\frac{L_g}{C_{iss}}} \quad (2)$$

where C_{iss} is the input capacitance from the MOSFET datasheet. It is evident how a correctly optimized layout can dramatically reduce the gate resistance requirement.
R_{gloop} is the total resistance in the gate charge loop:

$$R_{g_{loop}} = R_{down} + R_{gFET} + R_g \quad (3)$$

R_{down} is the internal pull down resistance of the IR11688 gate drivers; R_{gFET} is the internal gate resistance of the SR MOSFET and R_g is the external gate resistor. Typical values of R_{down} and R_{gFET} are good enough for this calculation.
Rearranging the equation gives:

$$R_g = R_{gloop} - R_{gFET} - R_{down} \quad (4)$$

3.4 Gate resistor and IC power loss calculation

To calculate IR11688 current consumption the gate charge of the synchronous MOSFETs needs to be determined. The secondary current initially flows through the body diode of each SR MOSFET, which will therefore be turned on in ZVS mode. In zero-voltage switching operation the MOSFET behaves like a constant capacitance load (C_{sync}) connected to the IC gate drive output because the variation of C_{sync} with V_{GS} is negligible.
The following diagram shows how the normal gate characteristics (Magenta) change when the switch is turned on at zero voltage (Blue). The gate plateau is effectively eliminated:

Design and selection of passive components

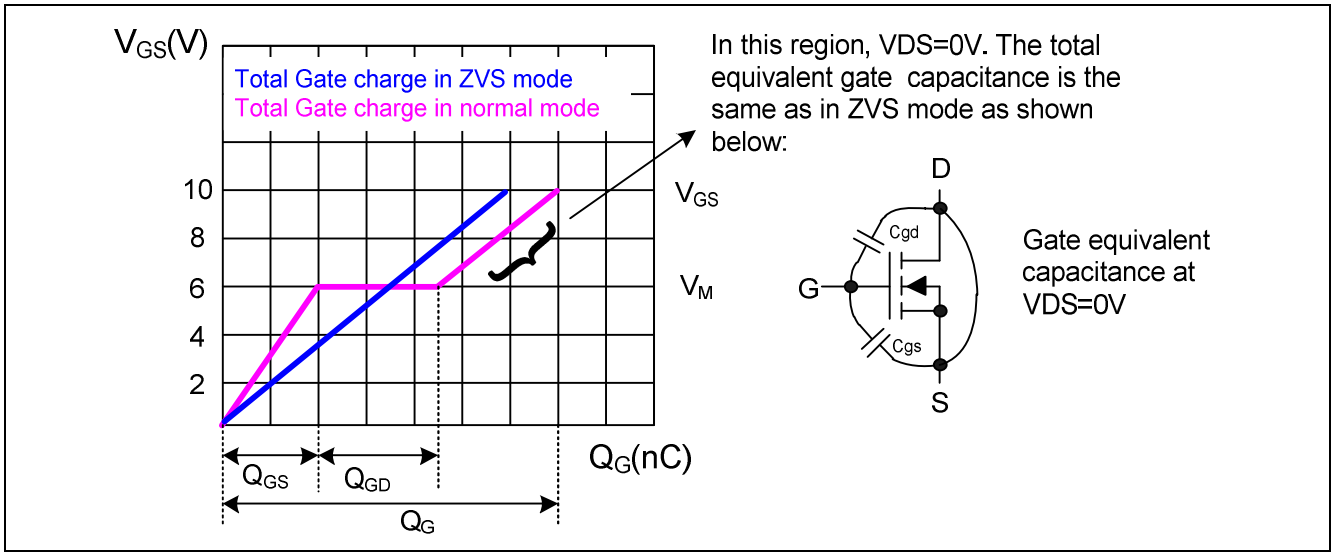


Figure 9 MOSFET gate equivalent capacitance in ZVS mode

$$C_{sync} = \frac{(Q_g - Q_{gd} - Q_{gs})}{Vgs - V_m} \quad (5)$$

Vgs is the gate voltage where Q_g, Q_{gd} and Q_{gs} are tested. In most datasheets it is specified as 10 V. V_m is the Miller plateau voltage. If two or more MOSFETs are connected in parallel, the above capacitance is multiplied by the number of devices.

The IC operating current can be calculated from the following equation:

$$I_{CC} = I_{QCC} + 2 \cdot f_{SW} C_{sync} V_{cc} + (0.285 \cdot V_{cc} - 0.425) \cdot 10^{-9} f_{SW} \quad (6)$$

where f_{SW} is the converter switching frequency. The first term is the quiescent current of the IR11688 in active mode. The second term is gate driver loss due to the synchronous MOSFET equivalent capacitance, while the third term accounts for the IC internal logic consumption during regular operation (the frequency dependent current requirements for the internal logic).

Not all the gate driver losses are dissipated in the IR11688. Losses are actually shared between the IC package, the external gate resistor and the MOSFET gate resistor. These resistances are in series in the gate driver loop, which means they will proportionally share the power dissipation.

The total power dissipated by the driver and the total gate resistance is calculated as follows. Calculations are based on a single channel.

$$P_{dr} = C_{sync} \cdot V_{cc}^{\ 2} \cdot f_{SW\max} \quad (7)$$

The driver buffer and the gate resistance will linearly share this power dissipation as described in the following relationship:

$$P_{R_g ext} = \left(\frac{R_g + R_{gFET}}{R_g + R_{gFET} + R_{Source}} + \frac{R_g + R_{gFET}}{R_g + R_{gFET} + R_{Sink}} \right) \cdot \frac{P_{dr}}{2} \quad (8)$$

Solving this equation with respect to $R_g$ext (which includes the external gate resistor R_g and the MOSFET internal gate resistance R_{gFET}), it is possible to determine the percentage of the total driving power dissipated in the gate resistor as a function of its value. Notice that in the IR11688 datasheet, pull up (r_{up})

and pull down (r_{down}) resistances are defined. For the above calculations, we use $R_{Sink} = 2r_{down}$ and $R_{Source} = 2r_{up}$ in order to allow for temperature drift and process variation.

The power loss in the IR11688 can now be calculated as:

$$P_{IC} = Vcc \cdot Icc - 2 \cdot P_{R_g ext} \quad (9)$$

It is clear that reducing supply voltage V_{CC} or increasing external gate resistor could effectively reduce SR controller IC power dissipation.

4 Other application information

4.1 MOT protection

At very light load or no load conditions, the secondary branch conduction period is likely to be less than the MOT period. If the SR is triggered then the MOSFET current will flow backwards from drain to source towards the end of the MOT period. This reverse current discharges the output capacitor causing energy to be transferred back to the transformer. Leakage inductance resonates with circuit capacitances resulting in ringing oscillations appearing at V_{DS} after the SR MOSFET turns off. This ringing can potentially cause the SR controller to mis-trigger and turn on the gate, creating more reverse current and subsequent multiple false triggering events as illustrated below:

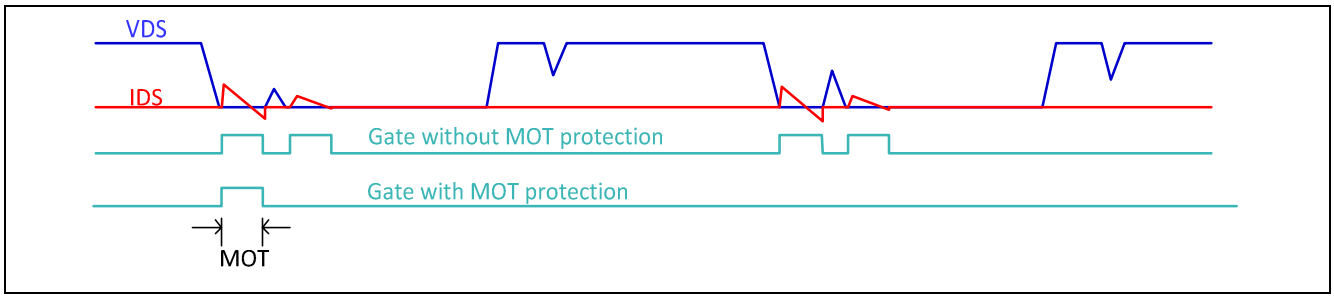


Figure 10 MOT protection waveform

The cycle-by-cycle MOT protection circuit of the IR11688 detects this reverse current condition and disables the following gate output pulse. This protection operates whether or not the gate drive is turned on so that a single event disables the SR until conduction has again been detected at the end of the MOT period. The pale blue waveforms in figure 10 compare SR gate drive behavior with and without MOT protection. The IR11688 continuously monitors load current and returns to normal operating mode once it has increased so that the conduction time is longer than the MOT.

Unlike the earlier IR11682, the IR11688 MOT duration is externally programmable via a resistor (RMOT) so that the user may set the trigger threshold at a desired load point below which the gate of IR11688 will be disabled by MOT protection. This function helps to reduce standby power losses.

Figure 11 shows a typical MOT cycle skipping waveform in an IR11688 based synchronous rectifier operating at light load. In this example the current conduction time in the SR is longer than the MOT. However since the output current is very low, the V_{DS} voltage drop of the MOSFET is already less than V_{TH1} at the end of MOT and consequently the IR11688 skips the next cycle. The body diode forward voltage drop during this next cycle is then sufficient to re-enable the gate output for the subsequent cycle. Under this borderline load condition, the IR11688 enables gate output every alternate cycle where the gate pulse width of each cycle is equal to the MOT. This operation is normal with the IR11688 and should not be cause for concern.

The IR11688 has independent MOT protection for each channel. It is therefore possible to for one channel to have MOT cycle skipping and the other channel to display normal operation, if channel 1 and channel 2 currents are not perfectly balanced.

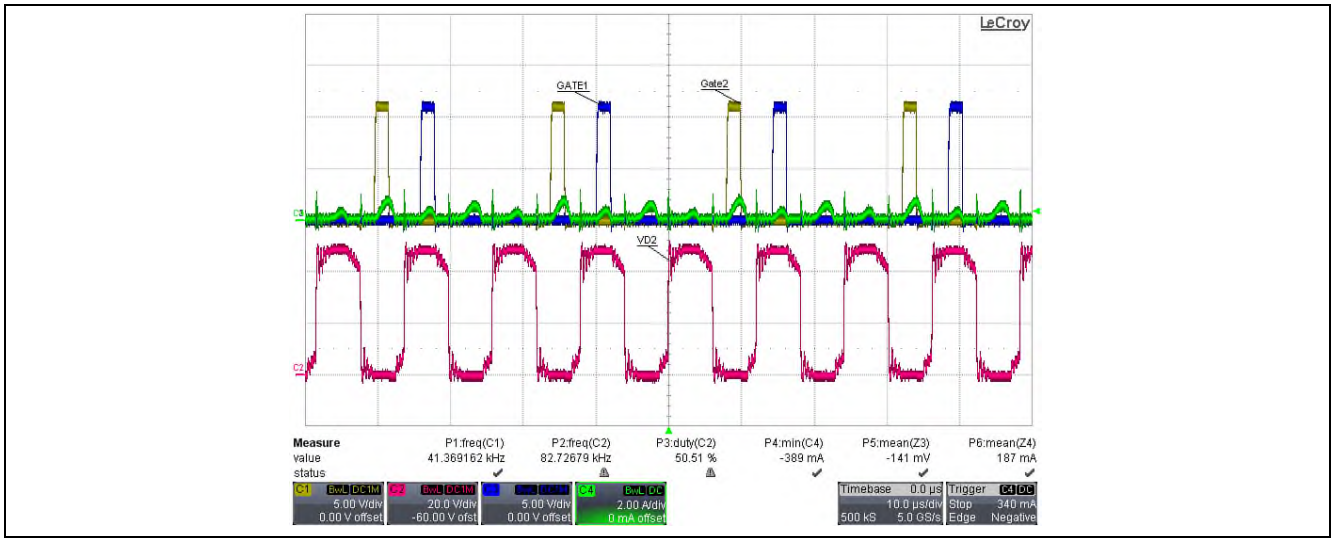
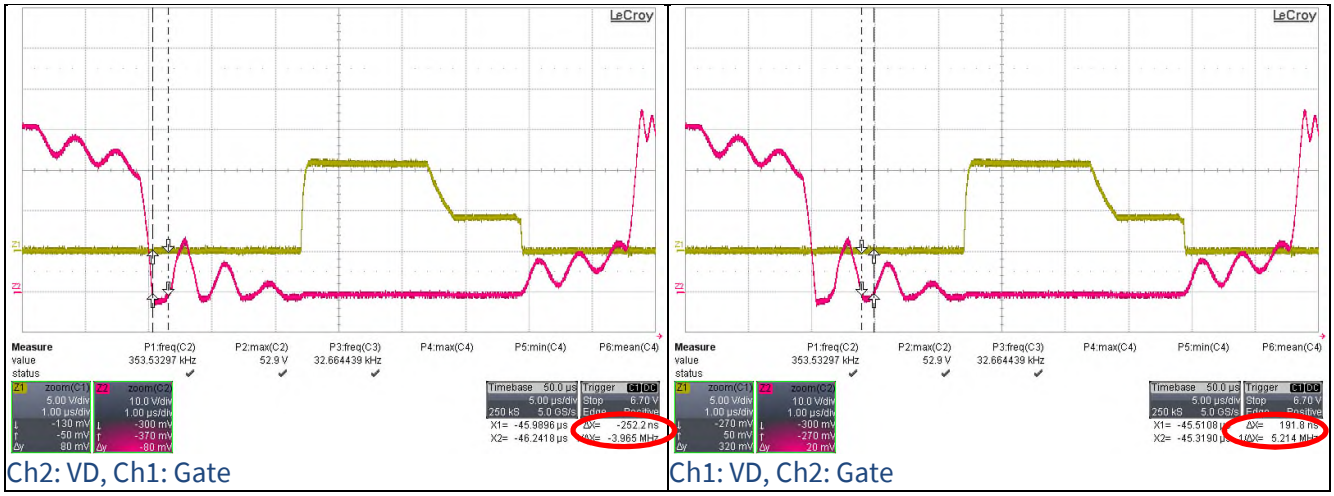


Figure 11 Waveform at light load with MOT pulse skipping

4.2 Turn-on blanking time and VD filter

As explained previously, the IR11688 incorporates leading edge blanking time and is therefore capable of preventing false triggering caused by ringing. The oscilloscope traces below show how the negative ringing is blanked so that the IR11688 only turns on the gate drive during the normal conduction period.



Ch2: VD, Ch1: Gate

Ch1: VD, Ch2: Gate

Figure 12 V_{DS} ringing at the beginning and the end of a switching cycle

The leading edge blanking time of the IR11688 is internally fixed. In cases where a longer filtering time is desired, a small additional RC delay may be added at the V_D input. To avoid bias current offsetting the V_D sensing voltage on the external resistor, the value of this resistor should not be higher than 1 kΩ.

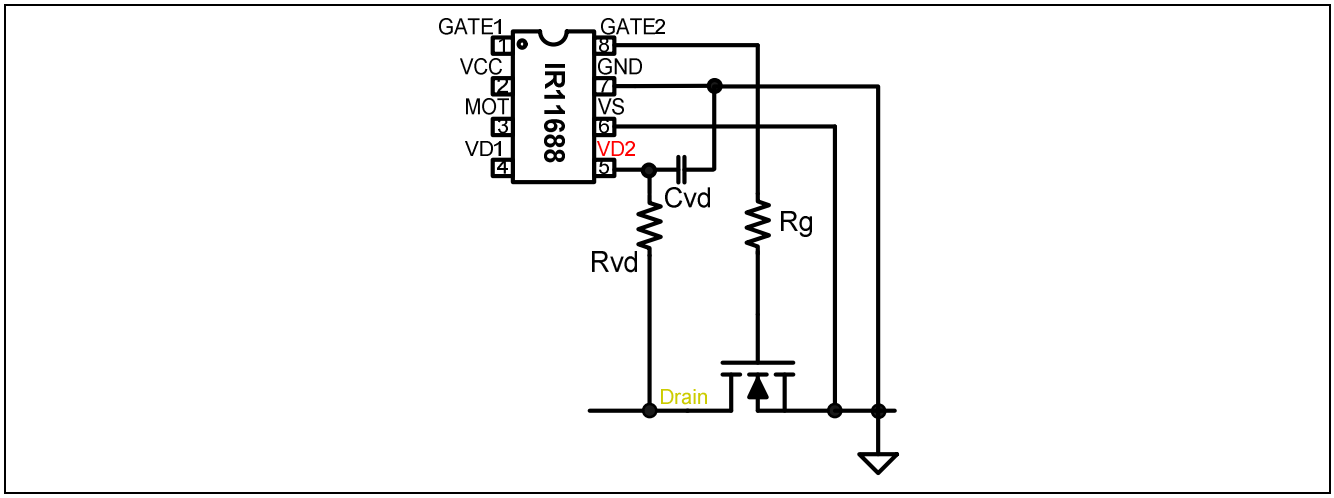


Figure 13 RC filter of VD pin

As shown in Figure 14, ringing with a 311 ns negative pulse width is filtered by a 1 kΩ + 47 pF RC network connected from the drain to the V_D pin greatly reducing the negative peak to prevent false triggering.

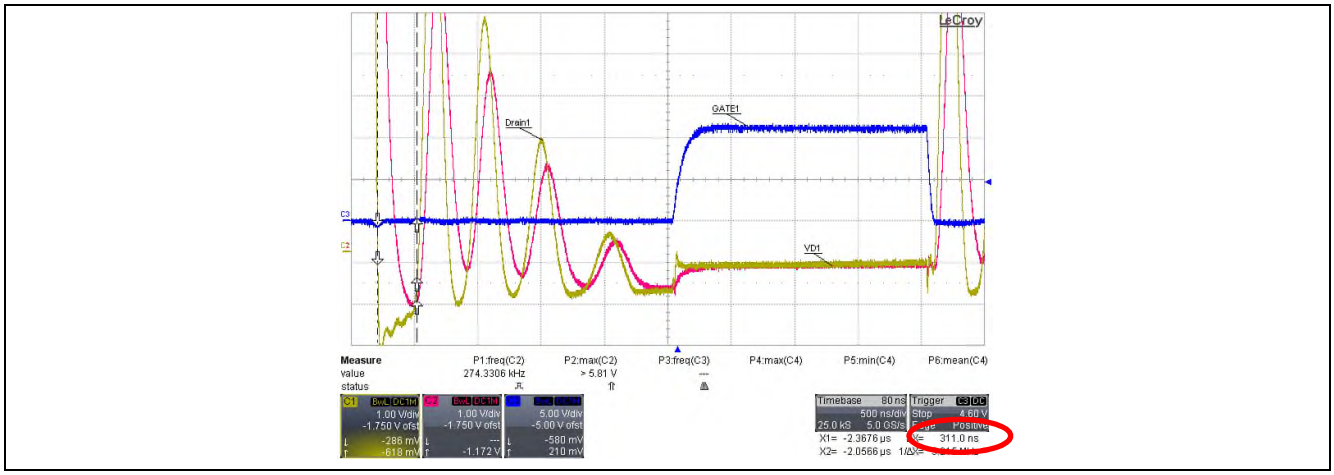


Figure 14 V_D waveform with 1 kΩ 47 pF filter (C1: Drain of SR MOSFET, C2: V_D waveform after RC filter, C3: Gate)

4.3 Early turn-off and regulation phase

As illustrated here, the parasitic inductance in series with the SR MOSFET tends to create a voltage drop resulting from the falling current. This would degrade the effectiveness of the SR controller voltage-sensing control technique by cancelling out drain to source voltage drop so that the SR controller switches off gate drive prematurely. Though the designer should always optimize the PCB layout as far as possible to minimize stray inductance, obtaining a true Kelvin contact to the MOSFET depends on the device package, die bonding and lead lengths. Through-hole packages such as TO-220 and TO-247 generally have larger stray inductances than surface mount packages like QFN, SO-8, or DirectFET. Even a small amount of inductance combined with a typical current slew rate can cause a voltage drop in the range of the IC's milli-volt switch off threshold levels (V_{TH1}). The effect is to trigger IC turn-off gate before drain current has fallen to V_{TH1}/R_{DSon} as in the ideal case.

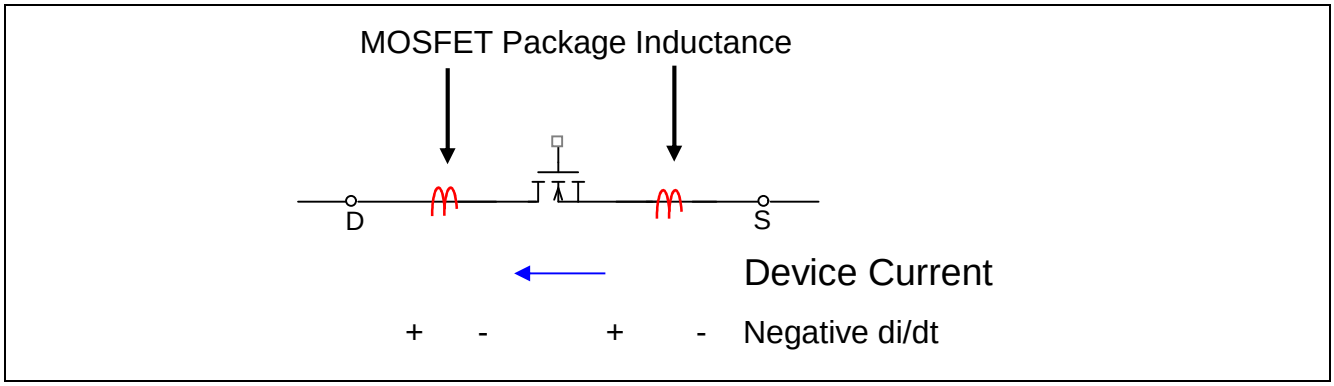


Figure 15 MOSFET package inductance

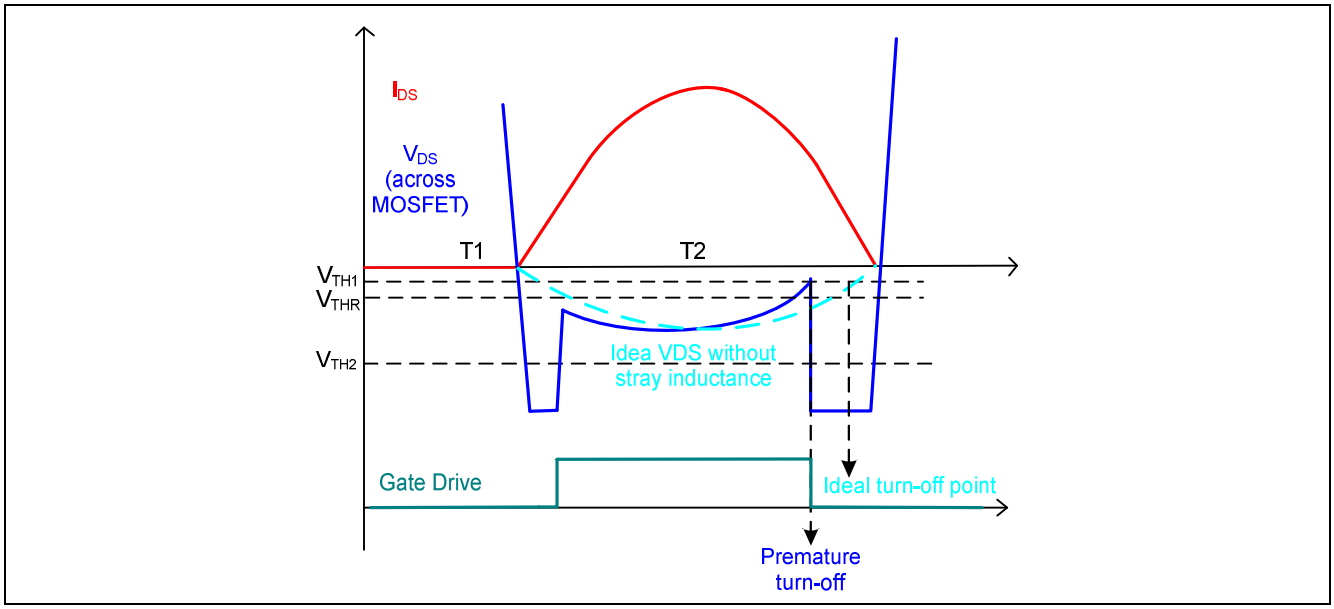


Figure 16 Premature turn-off waveform

Premature gate turn-off creates increased body diode conduction loss in the SR MOSFET since it is conducting through the body diode over a longer period. To overcome this problem, the IR11688 incorporates a gate voltage regulation function. In this way the SR MOSFET gate is pulled high only during the MOT period and after this the internal gate pull up is turned off so that the gate output enters a high impedance tri-state mode as previously mentioned. The gate voltage remains high due to the charge held by SR MOSFET equivalent gate capacitance. When the V_{DS} voltage increases to -40 mV, an internal slow discharge circuit is activated to gradually discharge the gate voltage. As a result the channel resistance of the SR MOSFET increases as the gate voltage decreases. The IR11688 stops discharging the gate voltage when V_{DS} falls below -50 mV. In this way V_{DS} is regulated between -40 mV and -50 mV. This function helps to compensate premature turn-off by maintaining a voltage at VD above the V_{TH1} switch off threshold down to very low current levels. This minimizes body diode conduction time at switch off and compensates for the effects of parasitic inductance.

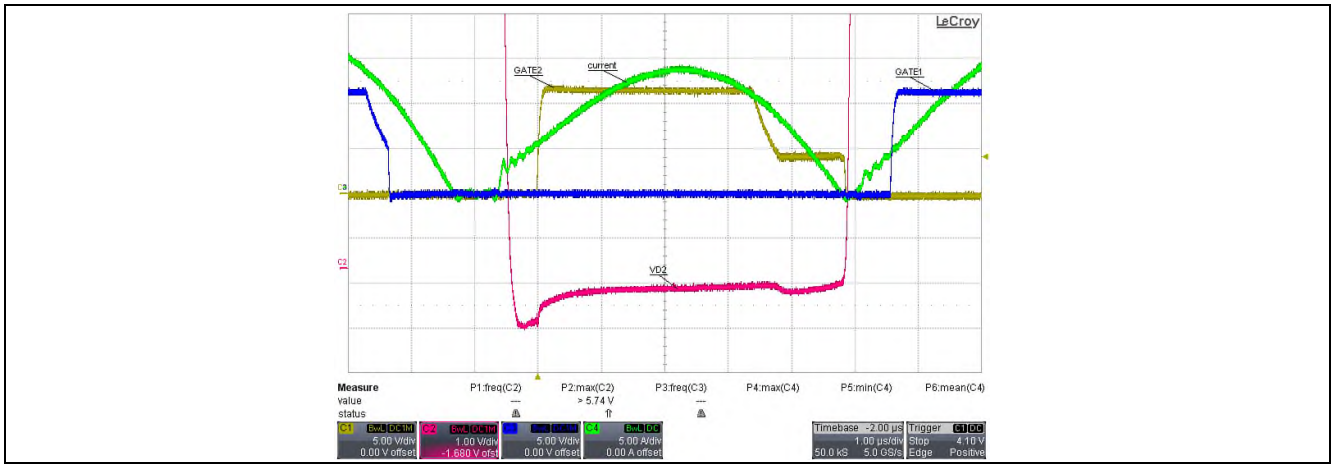
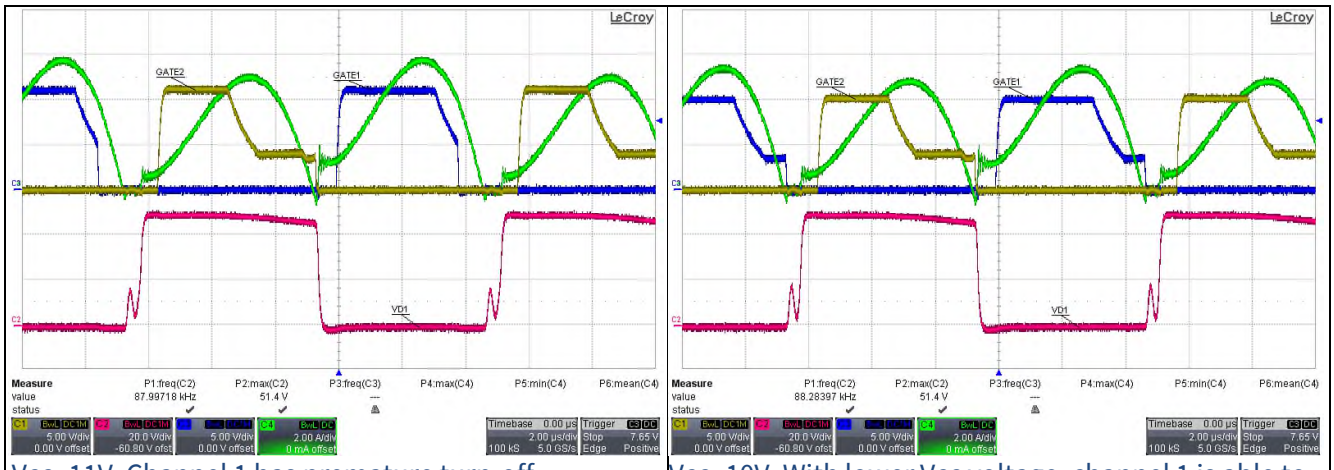


Figure 17 IR11688 regulation phase at turn-off

A MOSFET with a smaller Q_g will work more effectively with the IR11688. This is because a MOSFET with large Q_g may not able to utilize the regulation function and may therefore still have premature turn-off under a high di/dt condition. Figure 18 shows the gate 1 waveform, (blue trace) is discharged to 5.5 V in the regulation phase. Since MOSFET drain to source resistance does not change linearly with gate voltage, the channel resistance is not increased enough at 5.5 V Vgate to compensate the voltage offset created by stray inductance. Gate 1 is turned off when V_{DS} voltage reaches V_{TH1}. At this point MOSFET current is 4 A therefore significant body diode conduction loss occurs.

Reducing the V_{CC} supply voltage can improve the performance of the IR11688 when driving large MOSFET, since the initial gate drive voltage is limited to V_{CC}.

This is illustrated in following waveforms:



Vcc=11V. Channel 1 has premature turn-off.

Vcc=10V. With lower Vcc voltage, channel 1 is able to keep regulation phase.

Figure 18 IR11688 gate regulation phase at different V_{CC} values

4.4 Light load ripple

One common issue encountered in LLC resonant converters with synchronous rectification, is the light load ripple. In a light load condition, the synchronous rectifier can show higher output ripple due to the burst mode switching that results from the SR driver IC operating intermittently as shown in figure 19:

Other application information

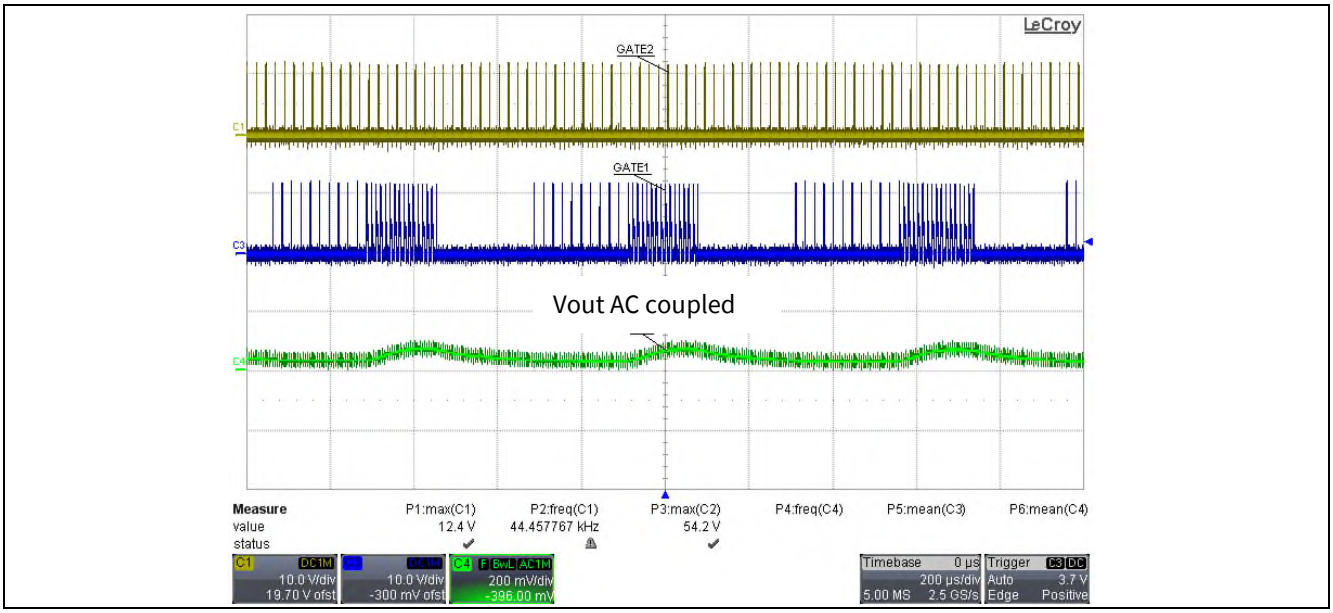


Figure 19 Light load ripple due to intermittent gate drive

This happens because of the sinusoidal shape of the output current in an LLC resonant converter. The current in the SR MOSFET always rises from zero to its peak in the first half of the conduction phase and then drops to zero in the second half of conduction phase. At light load the output current is too low to hold the V_{DS} voltage more negative than V_{TH1} at the end of the MOT time. The IR11688 will therefore turn-off the gate drive immediately after MOT has expired, leaving the body diode to take over and carry the current for the rest of the conduction phase.

At the boundary load condition, the output current causes V_{DS} to be right around the V_{TH1} threshold at the end of MOT the time. The SR controller sees short conduction pulses for a few cycles, and enters MOT protection disabling the gate drive. After conducting through the body diode for the next few cycles the output voltage drops since body diode voltage drop is higher than channel R_{DSon} voltage drop. Conduction time then increases slightly to recharge the output capacitor and the cycle repeats resulting in higher than normal output voltage ripple. Intermittent gate drive output of the SR controller only happens at the boundary condition and is inherent in any controller with MOT protection. If the load is reduced further, the IR11688 will stay in MOT cycle skipping mode or totally disable gate output. At higher load, the IR11688 is able to turn-on for the full conduction time in every switching cycle.

Other application information

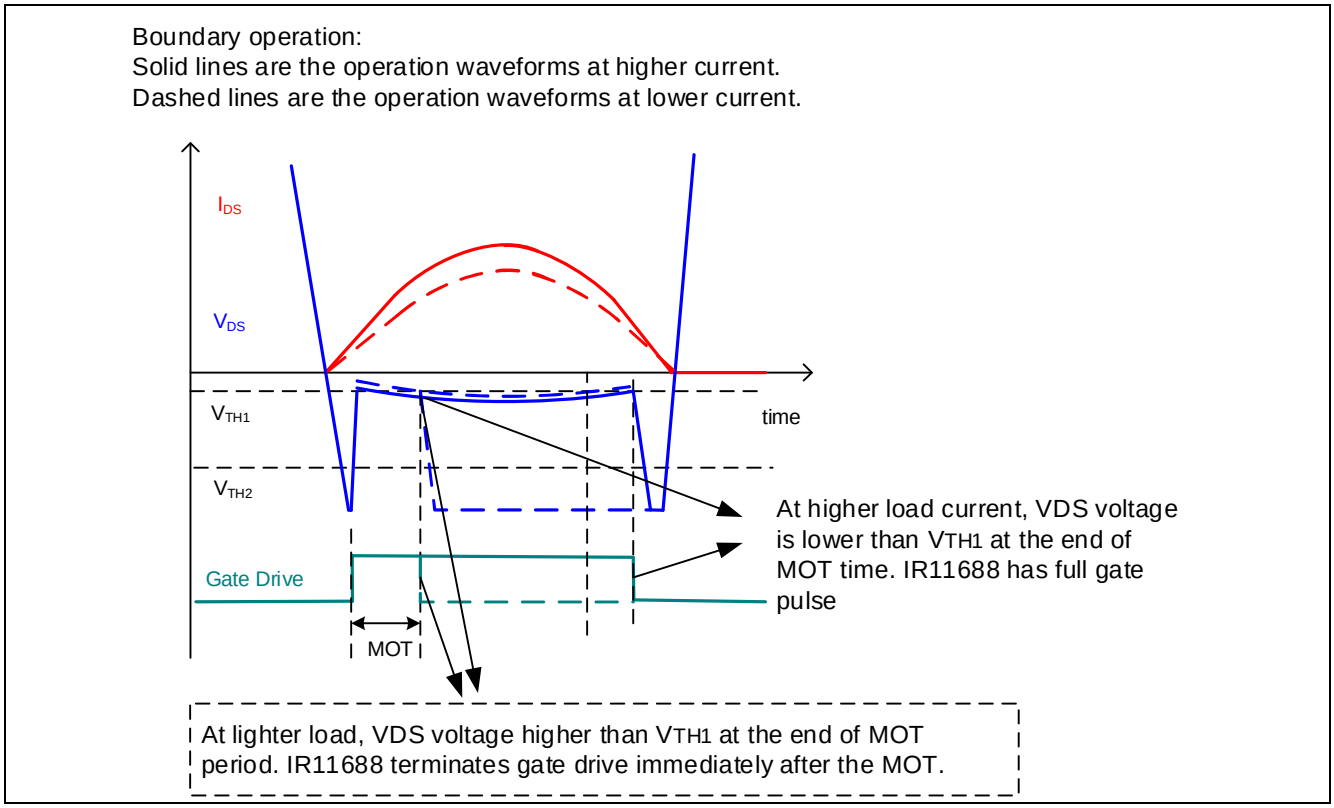


Figure 20 Light load ripple due to inconsistent gate drive

A solution is to set the MOT so that the boundary point will be at a current level as low as possible. At lower current output ripple can be managed to an acceptable level. To achieve this using earlier SR controllers such as the IR11682 it is necessary to add dynamic offset to the V_S pins in order to extend the effective minimum on time. However with IR11688 it can be done more easily by increasing the MOT resistor value to obtain the necessary minimum on time. The waveforms below show the same LLC converter at 1A load with MOT set to 1µs and 2 µs respectively. It can be seen that extending the MOT effectively brings the IR11688 into steady operation. As a design rule of thumb, it is suggested to set the MOT between 25% and 40% of the switching period at f_{SWmax}.

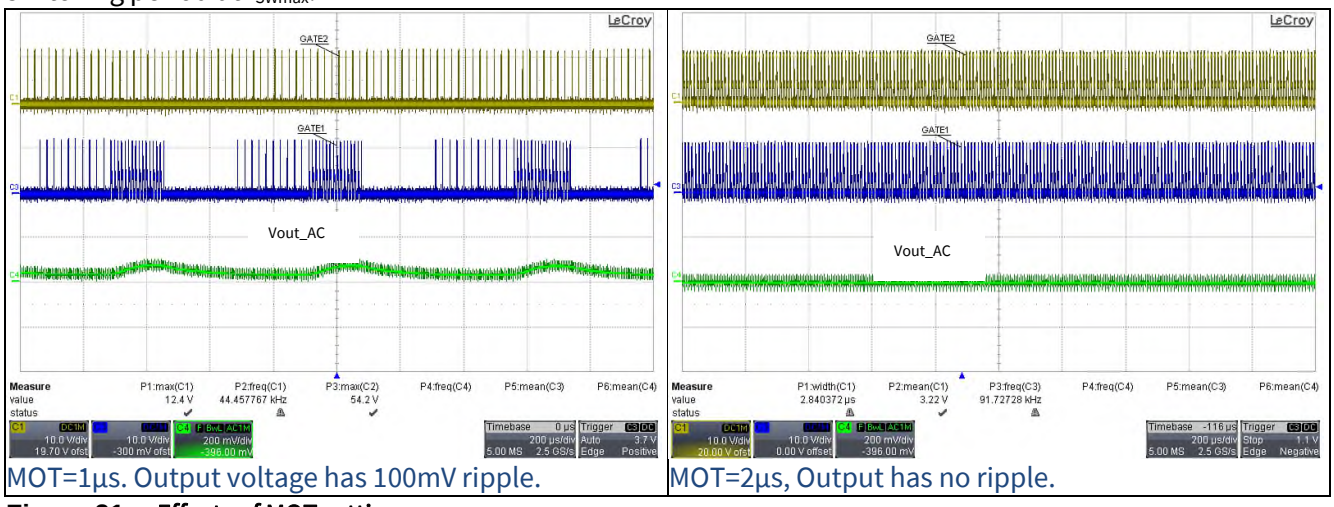


Figure 21 Effects of MOT setting

To fully eliminate this problem, it is suggested to disable the IR11688 at light load. This can be done by removing the V_{CC} supply.

4.5 Gate clamping circuit for logic level MOSFET

The IR11688 is able to directly drive logic level MOSFETs. However if the dv/dt appearing at the drain is too high and the MOSFET Miller capacitance is large, voltage spikes reaching the gate threshold can be coupled from drain to gate. If this occurs before the SR control IC Vcc supply has risen sufficiently for it to be fully biased (V_{CC}< 2 V), the gate drive does not have sufficient pull down to prevent possible switch on. It is advised to pay close attention to the gate voltage of the SR MOSFET during system power up. If gate voltages above 2 V are present, an external clamping circuit is recommended for logic level MOSFETs.

Figure 22 and 23 shows examples of clamping circuits. The PNP transistors are low voltage signal bipolar transistor (Figure 22); the clamp_FETs are logic level signal MOSFET (Figure 23); both circuits could provide sufficient pull down current at low V_{CC}. PNP clamping circuit will affect IR11688 regulation feature. Signal MOSFET clamping circuit is recommended if the regulation feature is desired.

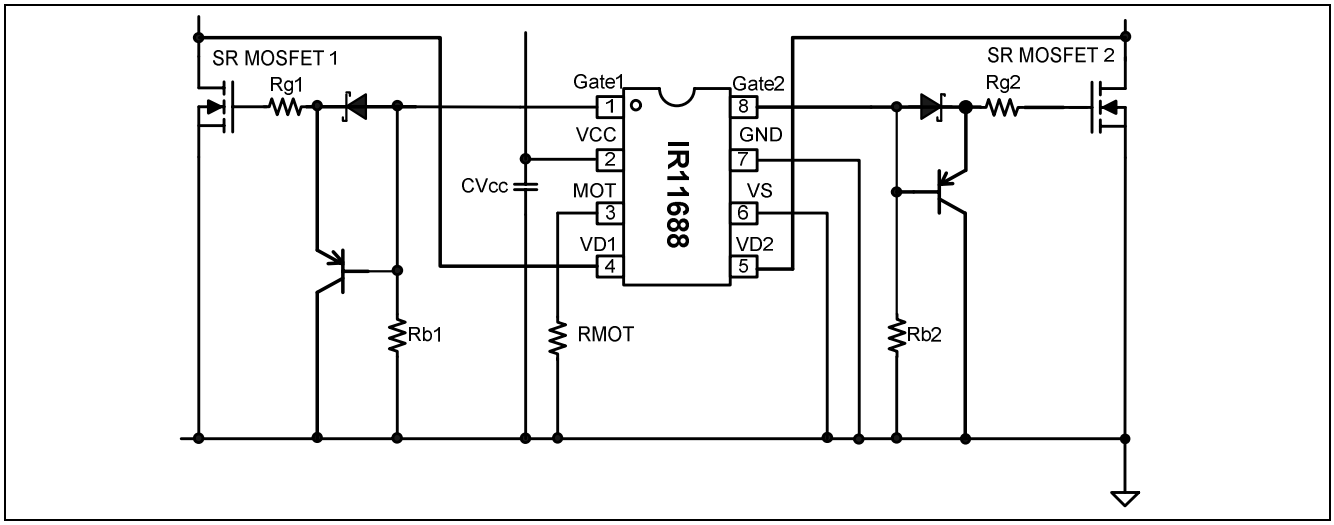


Figure 22 Gate clamping circuit for logic level MOSFET – PNP solution

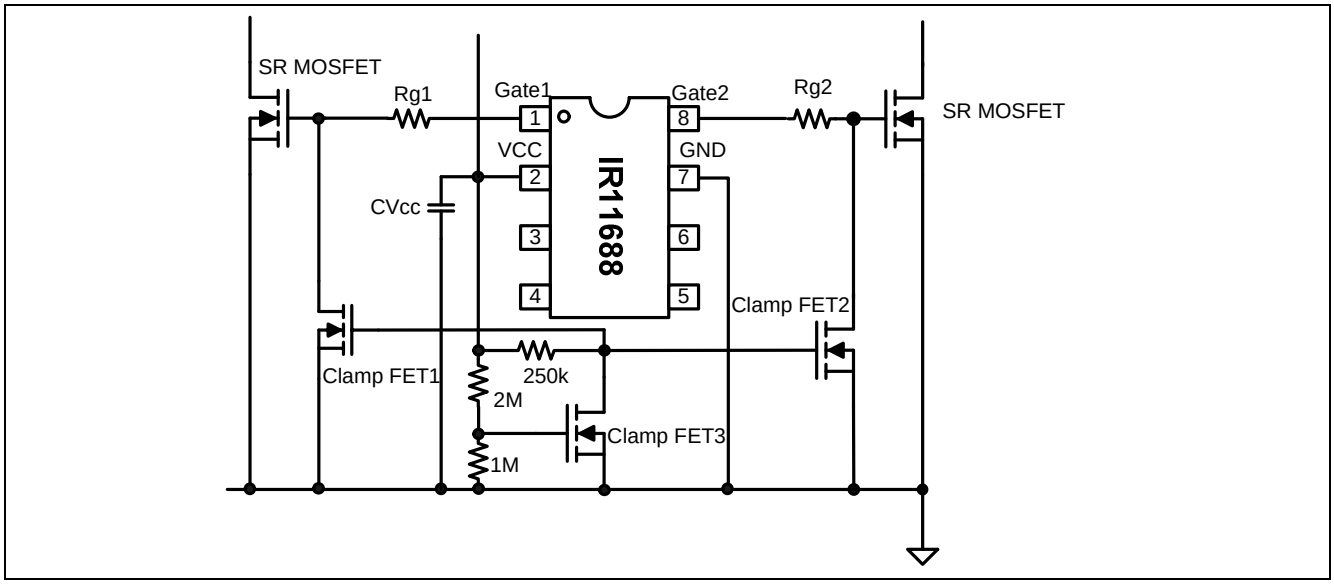


Figure 23 Gate clamping circuit for logic level MOSFET – signal MOSFET solution

5 SR MOSFET power loss calculation and MOSFET selection

The power loss in the SR MOSFET is the sum of conduction loss, switching loss, and gate driver loss.

The conduction loss of the IR11688 controlled synchronous rectifier can be broken down into body diode conduction loss, channel conduction loss, and regulation phase conduction loss. The conduction period is illustrated in Figure 24 where T_{b1} and T_{b2} are the body diode conduction phase, T_{con} and T_{reg} are the channel conduction phase.

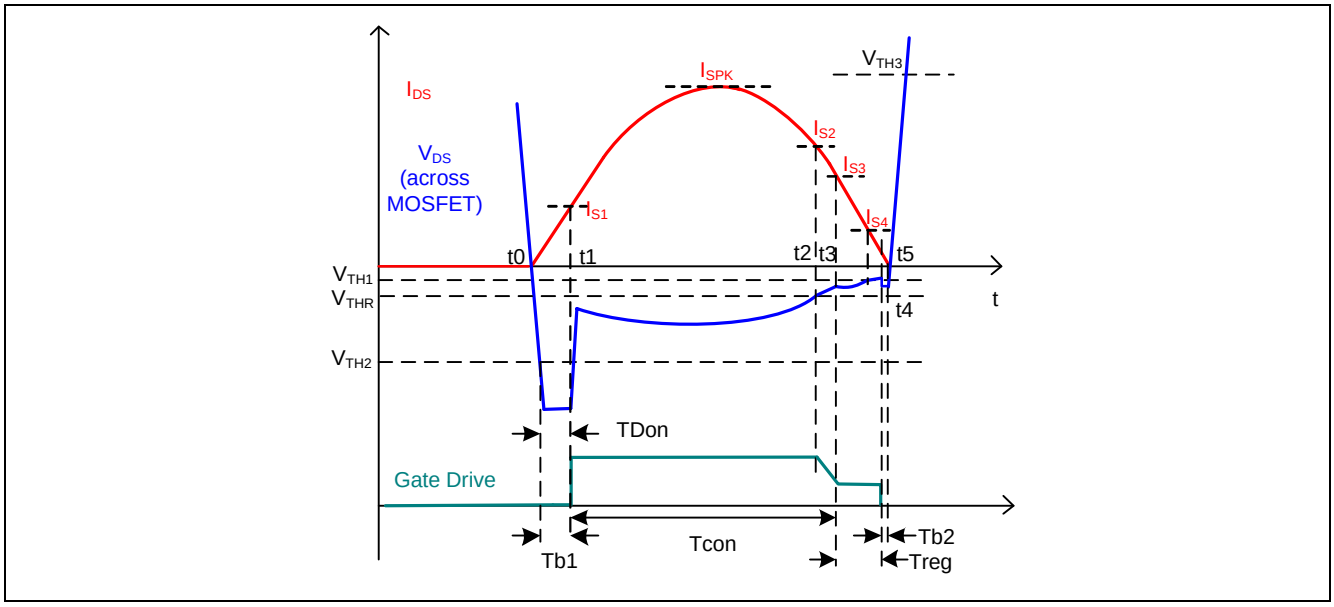


Figure 24 LLC sync rect waveform

5.1 Body diode conduction loss at turn-on

The power loss in the first body diode conduction phase can be calculated by:

$$P_{body1} = \frac{1}{2} \cdot T_{b1} \cdot f_{SW} \cdot V_F \cdot I_{S1} \quad (10)$$

T_{b1} is approximate the turn-on propagation delay of the IR11688 (T_{Don} in the datasheet). If additional turn-on delay is applied in the circuit or a large gate resistor is used, the additional turn-on delay and gate rising time should be considered in T_{b1}.

V_F is the body diode forward voltage drop. I_{S1} is the secondary current value at the time IR11688 gate turns on. I_{S1} can be estimated per the following equation:

$$I_{S1} = I_{SPK} \cdot \sin(2 \cdot \pi \cdot f_{SW} \cdot T_{b1}) \quad (11)$$

where I_{SPK} is the peak of secondary current, I_{SPK} is calculated by:

$$I_{SPK} = \frac{\pi}{2} \cdot Iout \quad (12)$$

and I_{out} is the average current of LLC converter.

The above calculation is based on an ideal sinusoidal current waveform when switching frequency is equal to resonant frequency. Actual secondary peak current is higher than this value when switching frequency is lower than resonant frequency (below resonant mode). In this case,

$$I_{S1} = I_{SPK} \cdot \sin(2 \cdot \pi \cdot f_r \cdot T_{b1}) \quad (13)$$

$$I_{SPK} = \frac{\pi}{2} \cdot Iout \cdot \frac{f_r}{f_{SW}} \quad (14)$$

Where f_r is resonant frequency of LLC converter. f_r is defined by resonant inductor L_R and resonant capacitor C_R. Please see details in appendix: transformer leakage inductance and modeling.

5.2 Conduction loss in regulation phase

Before calculating MOSFET channel conduction loss, it is necessary to first review the conduction loss generated during the regulation phase. As explained in section 4.3, parasitic inductance in the V_{DS} sensing loop creates voltage offset. The offset voltage generated by parasitic/stray inductance can be calculated by the secondary current di/dt slope and the package stray inductance of MOSFET (L_{STRAY}).

$$V_{OFFSET} = \frac{di}{dt} L_{STRAY} \quad (15)$$

The regulation phase starts at t2, where secondary current drops to I_{S2},

$$I_{S2} = \frac{V_{THR} + V_{OFFSET}}{R_{DSon}} \quad (16)$$

V_{THR} is the regulation threshold of the IR11688; the absolute value without a negative sign is used for this calculation.
In a normal SR conduction cycle, the regulation phase should happen during the second half of the sinusoid waveform, which is the falling slope. Thus the regulation phase starting time t_2 is calculated by:

$$t_2 = \frac{\pi - \arcsin(\frac{I_{s2}}{I_{SPK}})}{\pi \cdot 2 \cdot f_r} \quad (17)$$

At t2, gate voltage starts to be discharged by the IR11688. At time t3, the gate voltage is low enough to maintain the regulation of V_{DS} at -50 mV. The discharging time (t3 - t2) is determined by the SR MOSEFT equivalent SYNC capacitance C_{sync}, and the gate threshold voltage where drain-source resistance drops rapidly. As a general guide, the Vgs voltage that gives 2x of rated R_{DSon} can be used for the calculation (V_{GS2}). This voltage can be found in MOSFET datasheet in a plot of R_{DSon} vs. V_{GS}.

$$t_3 - t_2 \approx 150 \cdot C_{sync} \cdot \ln(\frac{V_{cc}}{V_{gs2}}) \quad (18)$$

$$t_3 \approx t_2 + 150 \cdot C_{sync} \cdot \ln(\frac{V_{cc}}{V_{gs2}}) \quad (19)$$

MOSFET current at t3 is then derived by:

$$I_{S3} = I_{SPK} \cdot \sin(2 \cdot \pi \cdot f_r \cdot t_3) \quad (20)$$

The power loss at regulation phase is:

$$P_{reg} = \frac{1}{2}(t_5 - t_3) \cdot f_{SW} \cdot I_{S3} \cdot (V_{THR} + V_{OFFSET}) \quad (21)$$

$$t_5 = \frac{1}{2 \cdot f_r} \quad (22)$$

5.3 Channel conduction loss

To simplify the channel conduction loss calculation, it is assumed that the MOSFET is turned on during the whole half of switching cycle. The RMS current in each branch of the synchronous rectifier is half of the peak current that calculated in the previous stage.

$$I_{SRMS} = \frac{I_{SPK}}{2} \quad (23)$$

$$P_{con1} = Isrms^2 \cdot R_{DSon} \quad (24)$$

R_{DSon} is MOSFET channel on state resistance. R_{DSon} (normally shown in the datasheet) at 25°C is approximately 1.5 times higher at Tj=100°C. Proper temperature coefficient should be considered in channel conduction loss calculation.

5.4 Body diode conduction loss at turn-off

If regulation phase works properly, the body diode conduction phase at turn-off is very short and the power loss is negligible.

5.5 Switching loss

The switching loss is different in DCM mode and CCM mode. For DCM, only the below-resonant operation at heavy load is of interest and is discussed here.

Figure 25 is a typical DCM waveform for switching below resonance (refer to Figure 2). V_S is the primary switching node voltage, VC_R is the primary resonant capacitor voltage, IL_R is the primary current, IL_m is the primary magnetizing current, I_{SR1} and I_{SR2} are the output current in each SR MOSFET and V_{DS1} is the Drain to Source voltage of SR MOSFET MSR1. At the end of each SR conduction cycle, the sinusoidal current reduces to zero and the SR MOSFET is turned off by the IR11688. When the switching frequency is below the resonant frequency, at the end of the conduction cycle the primary voltage has not changed polarity, therefore the SR MOSFETs of both channels remain in the off state and the V_{DS} voltage exhibits ringing oscillations.

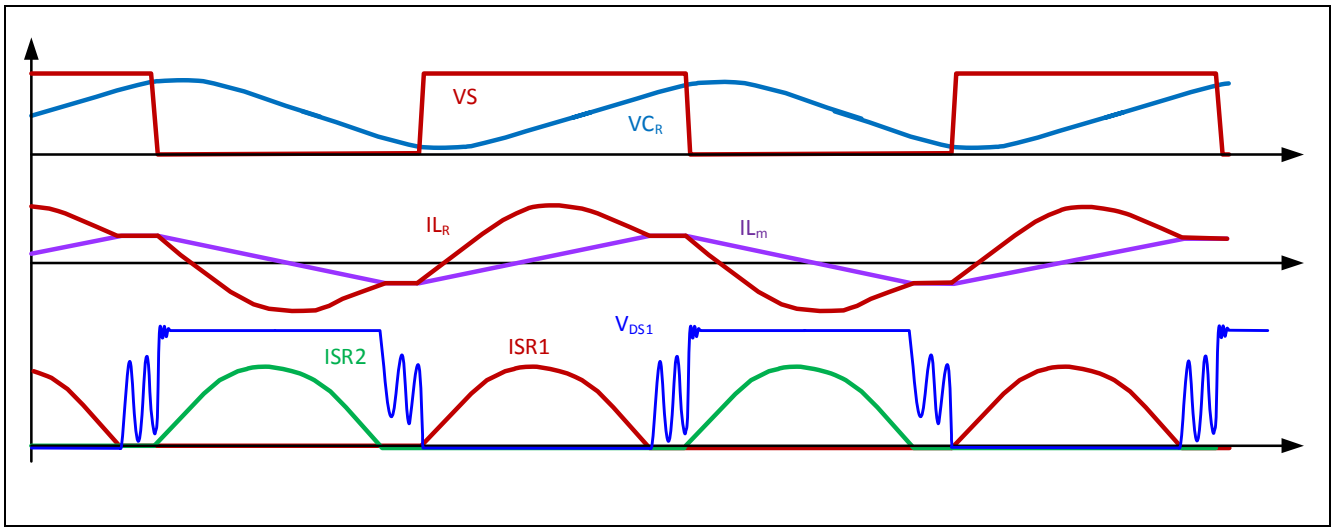


Figure 25 LLC below resonant DCM waveform

Figure 26 details the waveform of one SR cycle in below resonance DCM. From t0 to t1, power is delivered from transformer to load, t1-t0 duration equals to half of the resonant period. At t1, the resonant inductor current IL_R meets the transformer magnetizing current IL_m and secondary current reduces to zero. During t1 to t2, two resonant actions occur resulting from; firstly, primary side resonant inductor L_R, magnetizing inductance L_m resonating with C_R and secondly, the resonant inductor L_R resonating with secondary side SR MOSFET Coss. As C_R is much larger than SR MOSFET Coss, VC_R can be considered constant during t1-t2. The secondary high frequency oscillation during t1-t2 is defined by:

SR MOSFET power loss calculation and MOSFET selection

$$Fr3 = \frac{1}{2\pi\sqrt{L_R/n^2 \cdot (2 \cdot Coss_S)}} \quad (25)$$

Where $L_R = L_{R3}$ is the primary leakage inductance measured with all secondary winding shorted (refer to Appendix), *n* is transformer turns ratio and $Coss_s$ is Sync Rect MOSFET output capacitance. The equivalent resonant circuit is shown in Figure 27. The negative resonant current is defined by the body diode reverse recovery performance under the di/dt at t1. Please note the reverse recovery charge is usually much smaller than Qrr specified in the MOSFET datasheet as the di/dt and forward current in body diode are both smaller than datasheet test condition. During the resonance period, only small power loss drops on resistive components in the loop such as transformer ESR.

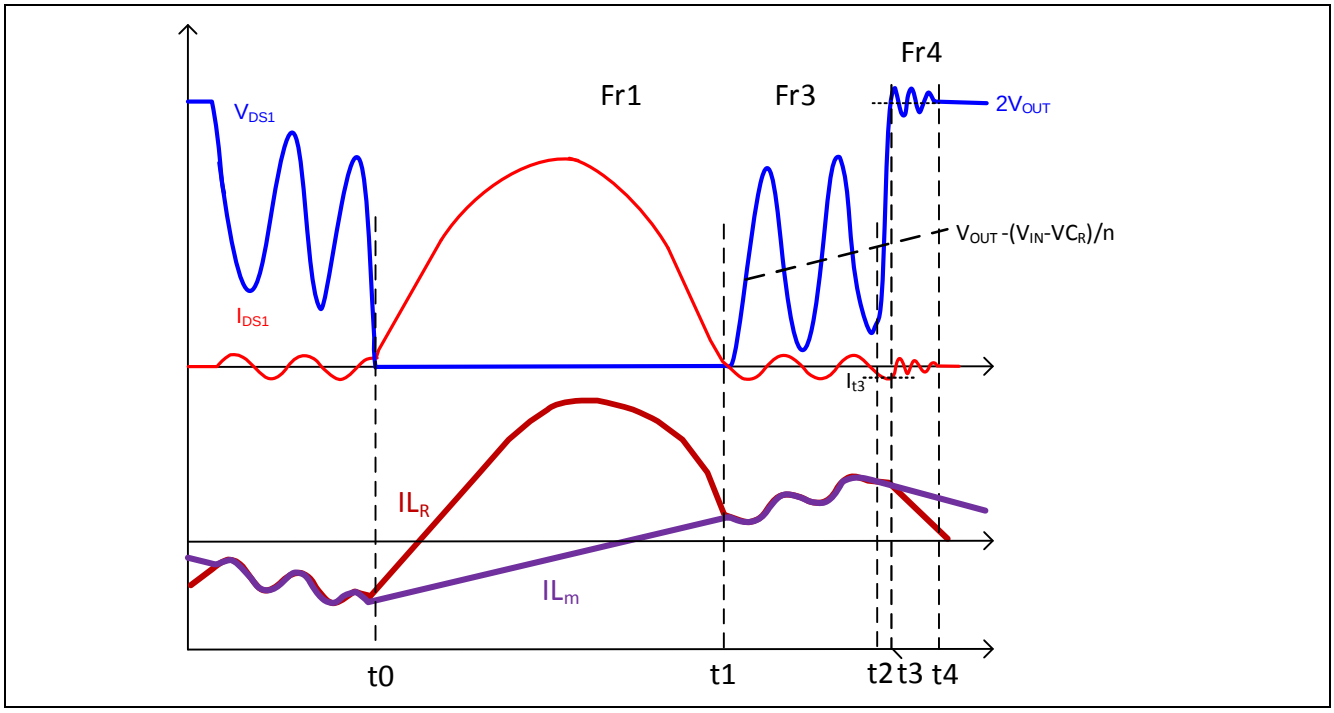


Figure 26 LLC DCM SR waveform of MSR1

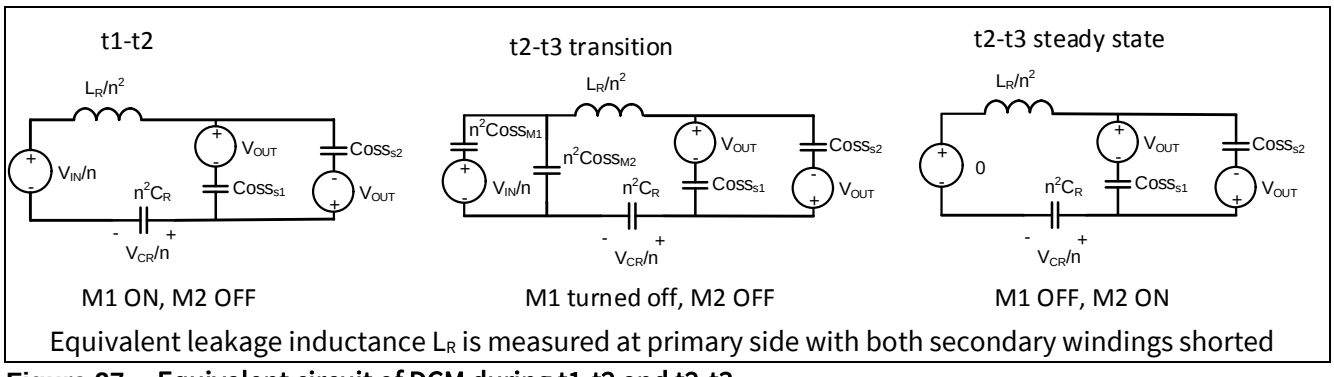


Figure 27 Equivalent circuit of DCM during t1-t2 and t2-t3

At t2, the primary high-side MOSFET M1 switch off, the transformer magnetizing current IL_m starts charging the parasitic output capacitor of M1, while discharging C_{OSS} of M2. IL_m can be considered as a constant current source during the transition. Primary dead-time can be calculated per IL_m and C_{OSS} of M1 and M2. The dead-time should be longer than the Coss charging/discharging time to guarantee ZVS operation. At time t2, the secondary V_{DS1} voltage could be anywhere between 0V and $2(V_{OUT}-(V_{IN}-VC_R)/n)$ depending on the resonant oscillation phase at t2. The I_{DS1} current at t2 always drops to negative due to negative di/dt applied. When the voltage at the V_S node drops to 0V, the secondary equivalent circuit in t2-t3 behaves very similarly

to the equivalent circuit in t1-t2. The only difference is the primary V_S node changes from V_{in} to 0 V (Figure 27). V_{DS1} rises due to the resonant components L_R and $Coss_s$ towards $2(V_{OUT}+VC_R/n)$. This resonant action is independent from the primary ZVS transition phase. It finishes as soon as V_{DS1} reaches twice the output voltage.

Once V_{DS1} of MSR1 exceeds twice the output voltage, MSR2 discharges to -0.7 V, the body diode of MSR2 starts to conduct current and so the IR11688 will turn MSR2 on. The transformer secondary winding voltage is clamped to V_{OUT} at t3, Fr3 resonance stops, and a higher frequency resonance Fr4 starts. The ringing frequency at t3-t4 is defined by:

$$Fr4 = \frac{1}{2\pi\sqrt{L_{paras}\cdot Coss_s}} \quad (27)$$

Here the parasitic inductance L_{paras} includes the transformer secondary leakage inductance between the two secondary windings L_{KS1-2} (refer to Appendix), stray inductance of secondary PCB trace, and MSR1 and MSR2 device package inductances.

Since $Coss_s$ of the SR MOSFETs are charged by the resonant circuit not by a voltage source, there is no Coss loss during the turn-off. However, the energy stored in the parasitic inductance creates voltage spikes on V_{DS}. The voltage spike is defined by the parasitic inductance, initial current in the parasitic inductance at t3 (I_{t3}) and Coss of the SR MOSFET. Reducing the length of the PCB power loop traces is always recommended to keep this voltage spike low.

$$V_{SPIKE} = 2\cdot V_{OUT} + \sqrt{\frac{L_{paras}\cdot I_{t3}^2}{Coss_s}} \quad (28)$$

The energy stored in parasitic inductance will dissipate in the SR MOSFET, transformer ESR and in the load. The switching loss in SR MOSFET is estimated:

$$P_{SW} < \frac{1}{2} L_{paras}\cdot I_{t3}^2 \cdot f_{sw}; \text{ } I_{t3} \text{ is SR current measured at } V_{DS}=2V_{OUT} \quad (29)$$

It worth mentioning, that MOSFET Coss varies with V_{DS} voltage. The $Coss_s$ value in equation 25 (t1-t2) is different to the $Coss_s$ in equation 27 (t2-t3). Please refer to the MOSFET datasheet to obtain the correct value from the capacitance plots.

CCM operation waveform is shown in Figure 28. In CCM operation, the switching frequency is higher than the resonant frequency, referred to as above resonance operation.

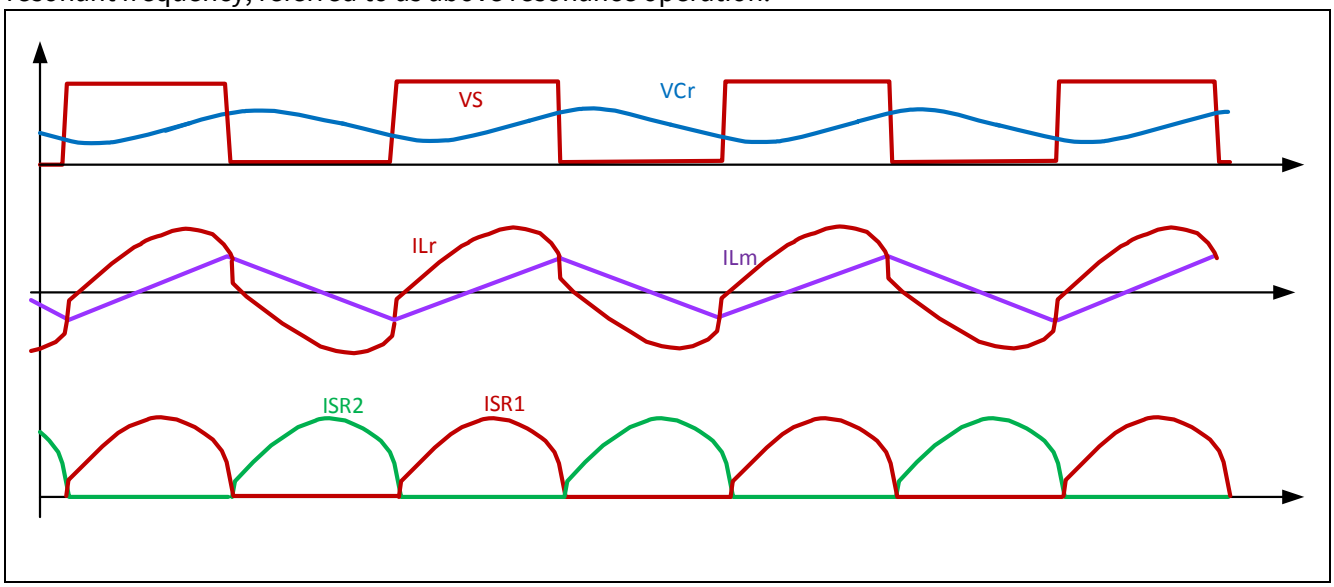


Figure 28 LLC CCM waveform

Figure 29 is the waveform of one SR cycle operating in CCM. From t0 to t1, power is delivered from the transformer to the load. At t1 the primary high-side switch M1 turns off then the switching node voltage V_S swings from V_{IN} to 0 V. The secondary SR current I_{D_CCM1} remains above zero, which depends on the level of

SR MOSFET power loss calculation and MOSFET selection

I_{D_CCM1}. The IR11688 may or may not turn off MSR1 at t1 so either the channel or the body diode of MSR1 conducts current. The transformer secondary voltage is still clamped to V_{OUT}. The whole V_S voltage swing (V_{IN}) is dropped across the resonant inductor L_R to generate negative di/dt. The di/dt slope during t1 to t2 is defined by:

$$\frac{di_{LR}}{dt} = \frac{V_{IN}}{L_R} \quad (30)$$

$$\frac{di_{DS}}{dt} = n \cdot \left(\frac{V_{IN}}{L_R} + \frac{n \cdot V_{OUT}}{L_m}\right) \quad (31)$$

The IR11688 will turn-off MSR1 as soon as the V_{DS1} voltage reaches V_{TH1}. The turn-off threshold can be calculated by the following equation.

$$ID_{CCM2} = \frac{V_{TH1} + \frac{di_{DS}}{dt} \cdot L_{STRAY}}{R_{DSon}} - \frac{di_{DS}}{dt} \cdot T_{Doff} \quad (32)$$

Where, T_{Doff} is IR11688 turn-off propagation delay.
It is worth mentioning that here the R_{DSon} could be larger than specified in the datasheet as the IR11688 would usually be in regulation mode during turn-off.

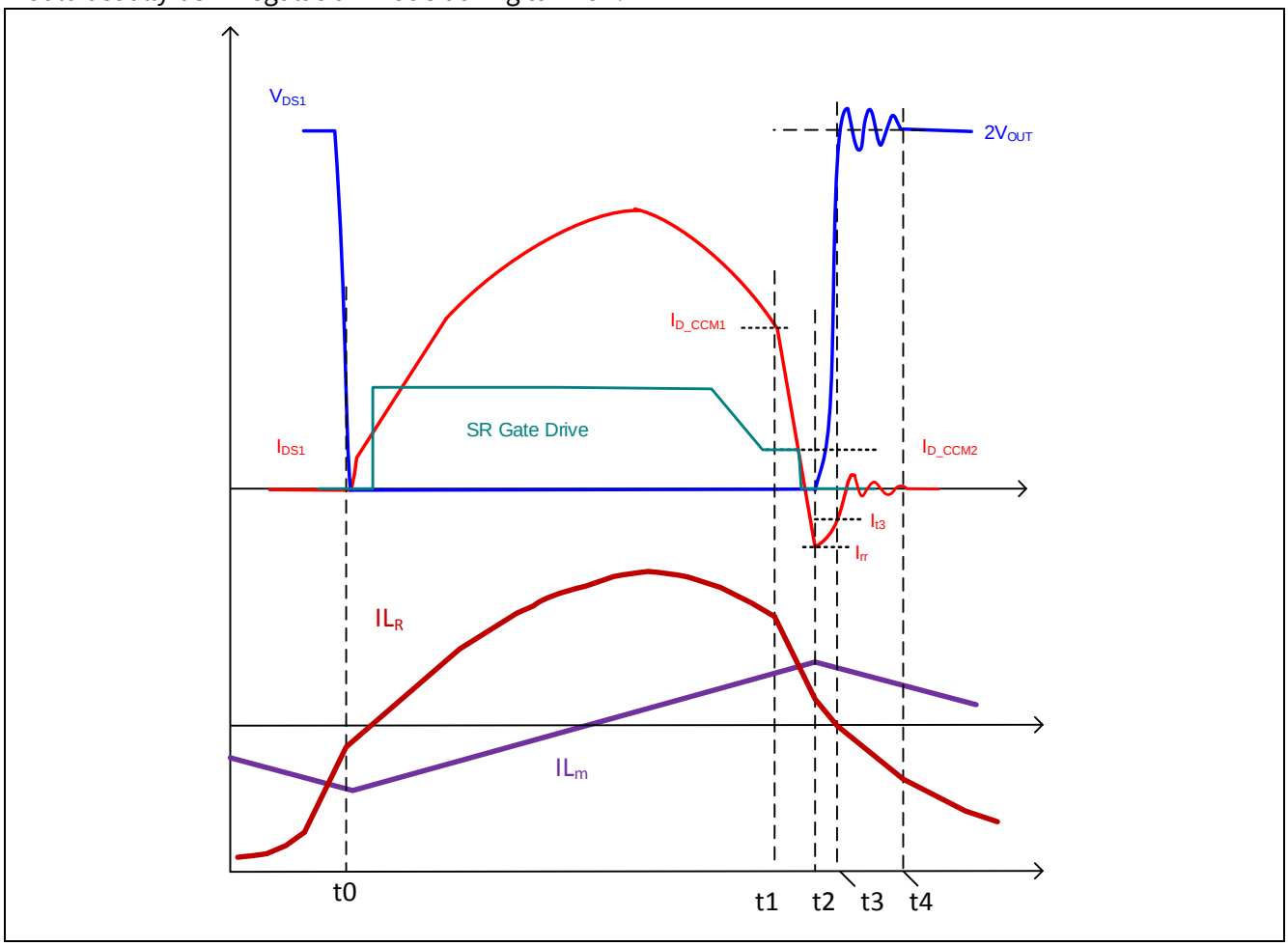


Figure 29 LLC CCM SR waveform of MSR1

When the MSR1 channel is turned off, I_{DS} current transfers to its body diode. The body diode will continue carrying current to negative I_{rr} until all the stored charges have been removed. At t2, the body diode starts blocking voltage. Irr is determined by initial current I_{D_CCM2}, the di_{DS}/dt @ t1-t2, and the V_{OUT} voltage. Again usually this value is not available in MOSFET datasheets as the application condition is different to the JEDEC test condition.

From t2 to t3, $Coss_s$ resonates with the equivalent leakage inductance L_R reflected to the secondary. The resonant frequency at t2-t3 is Fr3 (equation 25). V_{DS1} voltage rises towards $2V_{OUT}$. This is the same as in DCM mode. As long as V_{DS1} exceeds twice the output voltage, the opposite winding forces the counterpart SR MOSFET MSR2 to conduct current. Fr3 resonance then stops and Fr4 resonance begins. Energy stored in the parasitic inductance creates a voltage spike on V_{DS1}.

$$V_{SPIKE} = 2 \cdot V_{OUT} + \sqrt{\frac{L_{paras} \cdot I_{t3}^2}{Coss_s}} \quad (33)$$

The energy stored in the parasitic inductance will dissipate in the SR MOSFET, transformer ESR and in the load. The switching loss in SR MOSFET is estimated:

$$P_{SW} < \frac{1}{2} L_{paras} \cdot I_{t3}^2 \cdot f_{sw}$$; I_{t3} is SR current measured at $V_{DS}=2V_{OUT}$ (34)

5.6 Gate charge loss

The total gate driver loss is discussed in section 3.4. P_{Rgext} is used to calculate the gate drive loss dissipated in the MOSFET:

$$P_{R_g FET} = \frac{R_{gFET}}{R_g} P_{R_g ext} \quad (35)$$

R_{GFET} is the internal gate resistance of the SR MOSFET and R_G is the external gate resistor.

Total power loss in the SR MOSFET is therefore:

$$P_{FET} = P_{body1} + P_{reg} + P_{con} + P_{sw} + P_{RgFET} \quad (36)$$

5.7 MOSFET selection guide

In LLC application, both turn-on and turn-off of SR MOSFET are in ZVS and are nearly in ZCS. Coss is charged by resonant circuit, not by voltage source. Conduction loss dominates and switching loss is minimal. The key parameters that affect performance are R_{DSon} and Qsync. Usually lower R_{DSon} results in lower conduction loss. However, keep in mind IR11688 control scheme is based on V_{DS} sensing. Lower R_{DSon} would trigger IR11688 switch-off MOSFET at a higher current level and lead to higher conduction loss due to body diode. As rule of thumb, it is suggested choosing R_{DSon} at around 50 mV/Iout.

6 PCB layout guidelines and examples

IC placement

Due to the nature of the control based on fast and accurate voltage sensing, it is essential to lay out the circuit keeping the IR11688 as close as possible to the SR MOSFETs. As a general guideline, the physical distance between the two devices should not exceed 10 mm (0.4 inches).

IC decoupling capacitor

The key element to properly decoupling the IC is the physical location of the V_{CC} capacitor and its connections to the power terminals. In order for this capacitor to provide effective filtering, it must be located as close as physically possible to the V_{CC} and COM pins and connected through the shortest available path.

Gate drive loop

Minimal gate drive loop will reduce requirements for damping and enhance system robustness. Gate loop inductance plays a major role in damping requirements. Once layout is finalized, then a “rule of thumb” estimation consists of measuring the physical loop trace length, assuming each millimeter (1 mm = 39.37 mils) to add 1 nH of inductance. Other methods include measurement (low frequency RCL meters or current slope for a given voltage pulse) or FEM simulations.

MOT resistor

The MOT resistor should be placed as close as possible to the MOT pin and GND pin. It should use a separate signal ground trace star-connected to the GND pin.

V_S connection

V_S pin is the differential sense pin for internal V_{DS} comparators. This pin should be Kelvin connected to the Source of SR MOSFETs. If the two SR MOSFETs are apart from each other, connect V_S to the Source of channel 2 MOSFET. Avoid connecting V_S directly to GND pin (pin7).

PCB layout guidelines and examples

Double layer board layout examples are shown in the following figures:

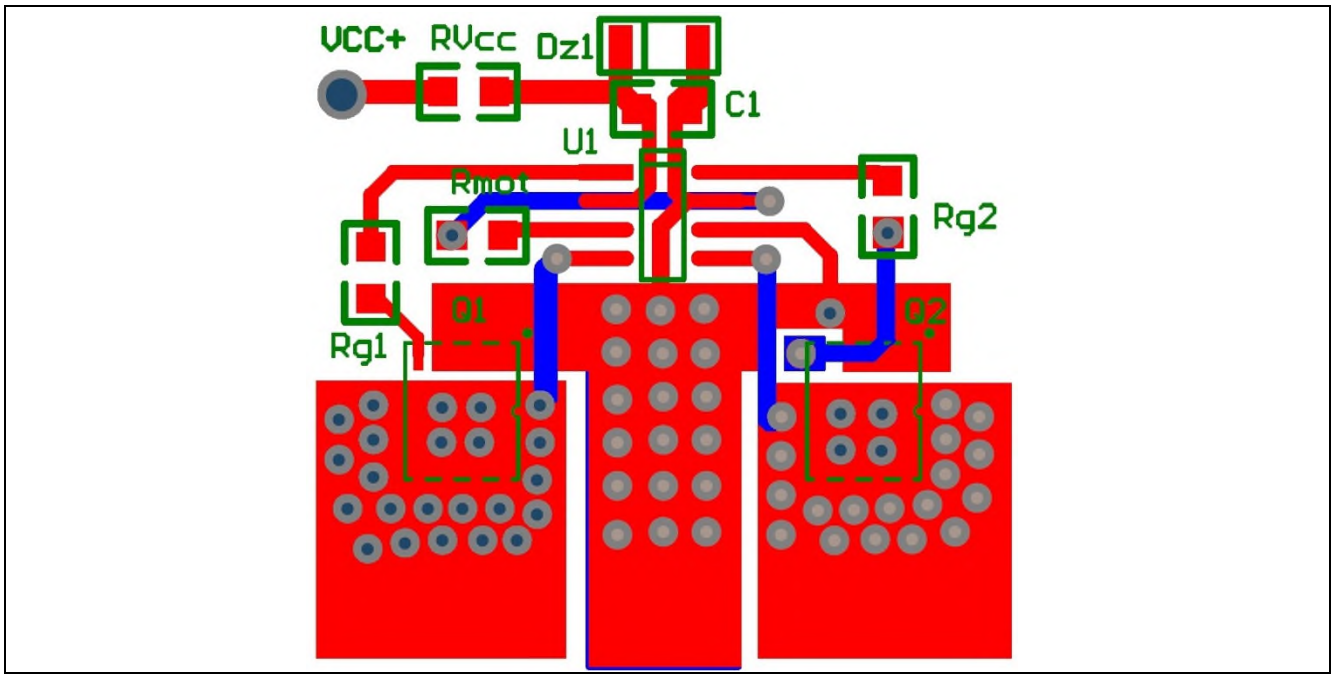


Figure 30 Single layer layout example with QFN MOSFET

Thermal vias are added to the QFN package to transfer heat from the top of PCB to the bottom layer.

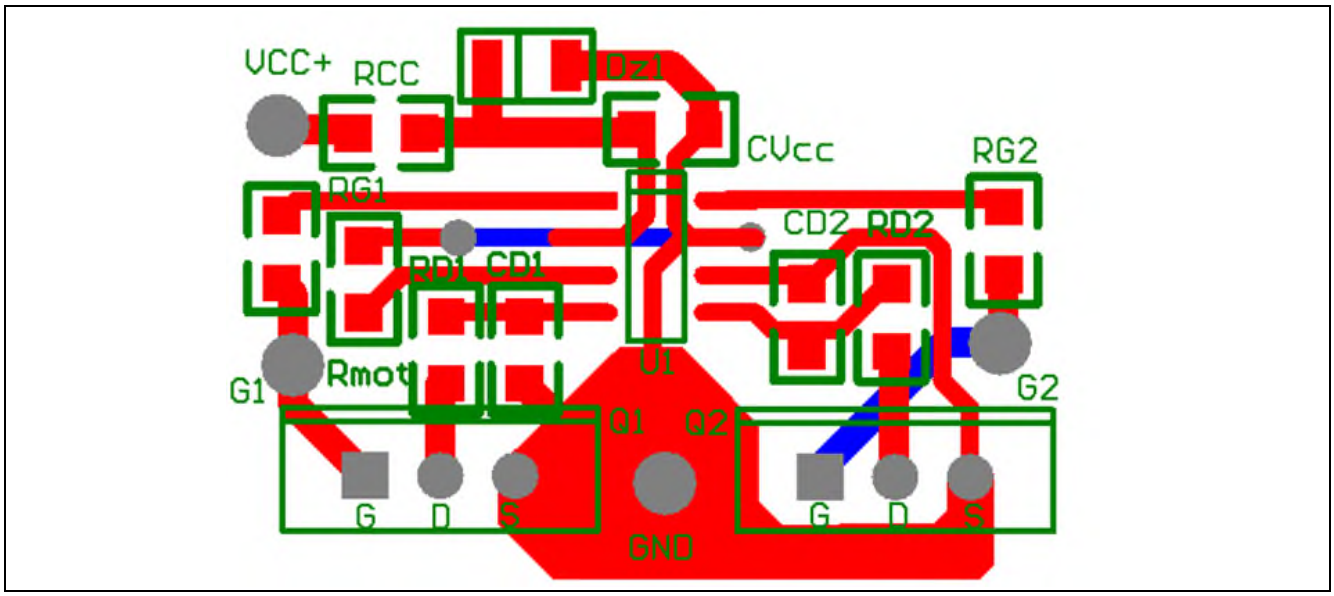


Figure 31 Single layer PCB example with TO-220 MOSFET

Add RC filter to VD pin when necessary to avoid DCM ringing false trigger IR11688

7 Appendix: Transformer leakage inductance and modeling

The physical model of a transformer with one primary winding and two symmetrical secondary windings (i.e. center-tapped secondary) is shown as Figure 32. Lm is transformer magnetizing inductance, L_{KP} is transformer primary leakage inductance, L_{KS1} and L_{KS2} are transformer secondary leakage inductance. Leakage inductance indicates flux is not coupled between primary and secondary.

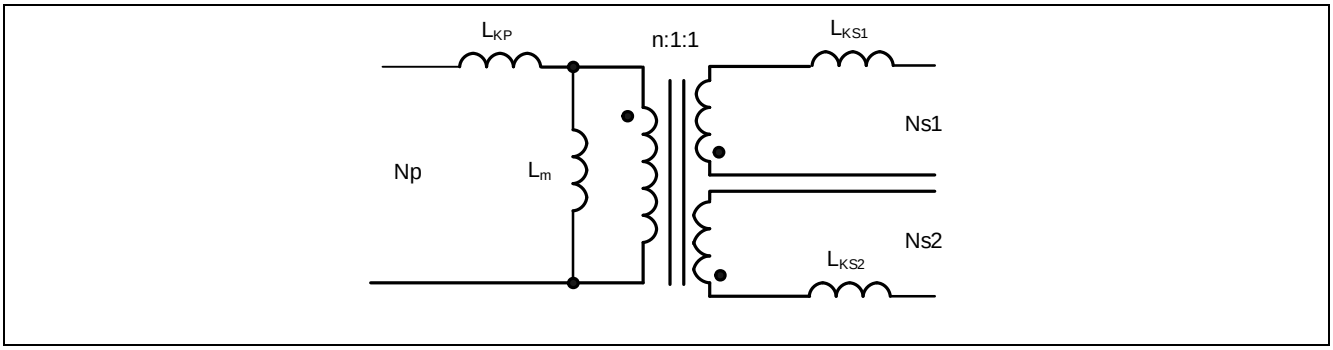


Figure 32 Transformer model

Figure 33 is a typical LLC circuit with simplified transformer model. L_R is resonant inductor and C_R is resonant capacitor. L_R and C_R define resonant frequency Fr1.

$$F_{r1} = \frac{1}{2\pi\sqrt{L_R \cdot C_R}}$$

L_R could be an external inductor or in many cases the leakage inductance of transformer. Here to simplify the statement, we take the second scenario: the resonant inductor is purely contributed by transformer leakage inductance.

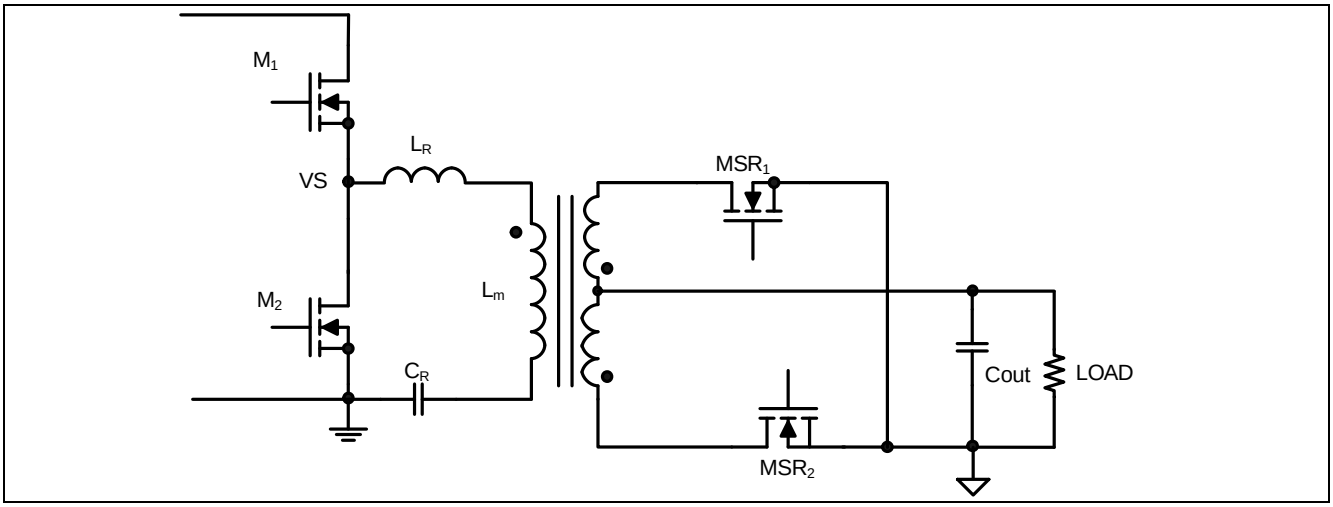


Figure 33 Typical LLC circuit

It is a general practice that leakage inductance is measured at the primary winding terminals with all secondary windings shorted. This leakage inductance includes the physical primary leakage inductance L_{KP} and physical secondary leakage inductance that reflected to primary. As mentioned, the leakage inductance is usually measured with all secondary windings shorted. This common practice however is not accurate and introduces error to the resonant circuit design.

Take the power delivery phase as an example. It happens when one secondary winding is conducting current; illustrated as Figure 34 (a). For AC analysis, output capacitor is considered short circuit. So we have

Appendix: Transformer leakage inductance and modeling

one secondary winding Ns1 in short and the other secondary winding Ns2 open. From the terminal of Np, it sees Np leakage inductance L_{KP}, in series with magnetizing inductance L_m, which is in parallel with reflected Ns1 leakage inductance n^2L_{KS1}. Please refer to Figure 34 (b). This is the actual inductance that resonant with C_R and creates sinusoid current shape. Thus the correct measurement of primary leakage inductance should be: measure primary winding inductance with only one of the secondary winding shorted.

$$L_{R1} = L_{KP} + \frac{L_m \cdot n^2 \cdot L_{KS1}}{L_m + n^2 \cdot L_{KS1}}, \text{ Np inductance when Ns1 is shorted}$$

$$L_{R2} = L_{KP} + \frac{L_m \cdot n^2 \cdot L_{KS2}}{L_m + n^2 \cdot L_{KS2}}, \text{ Np inductance when Ns2 is shorted}$$

The two leakage inductance L_{R1} and L_{R2} could be identical if the two secondary windings are exactly symmetric in physical location and size. If they have the same coupling to primary, we will get L_R=L_{R1}=L_{R2}. In reality, it is always difficult to put secondary windings symmetric. Then each secondary winding will have its own resonant frequency in its active half cycle. This could result in unbalance current in two secondary windings. The resonant frequency Fr1 is defined by:

$$F_{r1\_1} = \frac{1}{2\pi\sqrt{L_{R1} \cdot C_R}}$$

$$F_{r1\_2} = \frac{1}{2\pi\sqrt{L_{R2} \cdot C_R}}$$

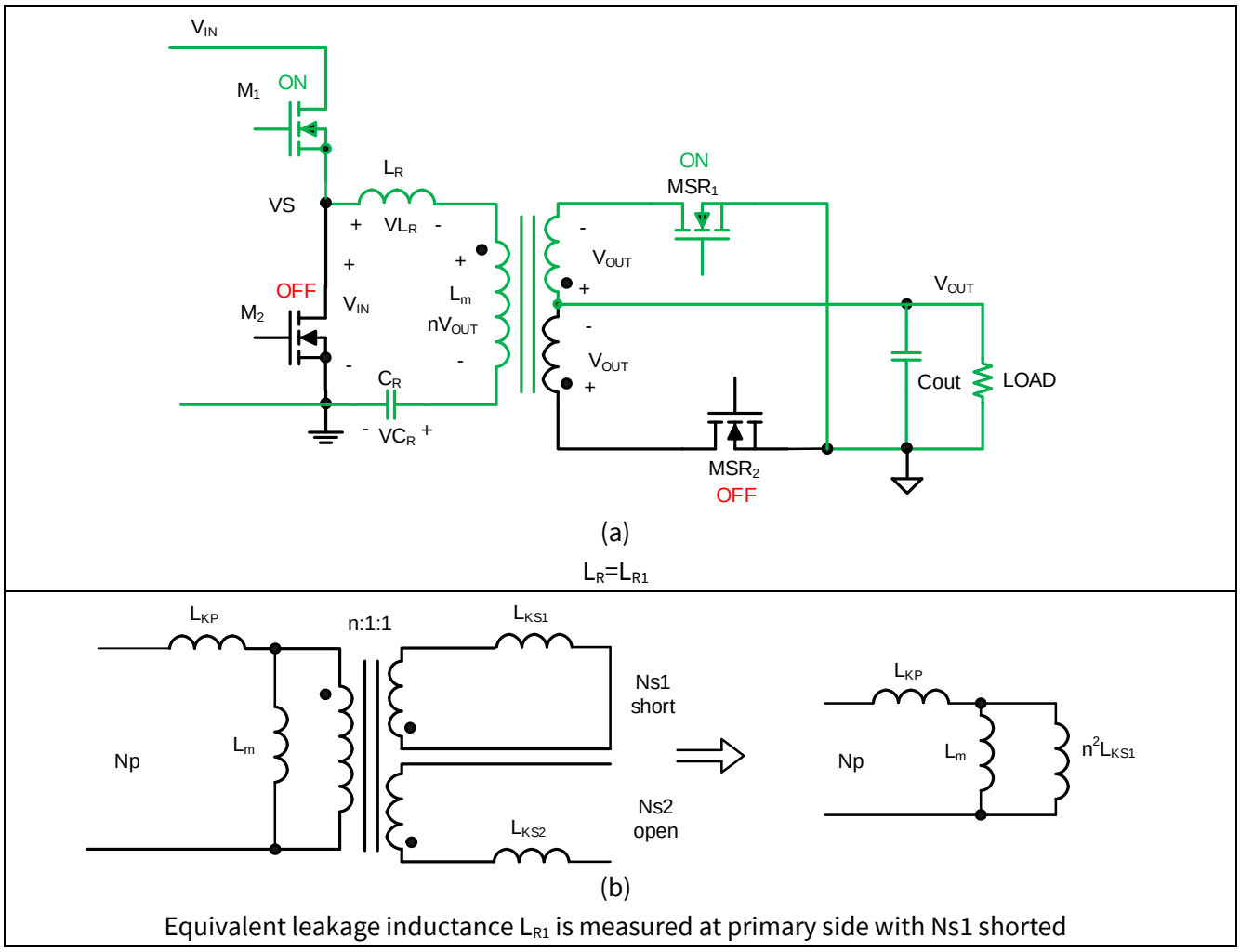


Figure 34 Equivalent transformer model in resonant (one secondary winding in conduction mode)

The following equations can be used to calculate each of the physical inductance in Figure 32.

Appendix: Transformer leakage inductance and modeling

$L_P = L_{KP} + L_m$, measure primary inductance with all secondary windings open

$L_{R1} = L_{KP} + \frac{L_m \cdot n^2 \cdot L_{KS1}}{L_m + n^2 \cdot L_{KS1}}$, measure primary inductance with Ns1 short

$L_{R2} = L_{KP} + \frac{L_m \cdot n^2 \cdot L_{KS2}}{L_m + n^2 \cdot L_{KS2}}$, measure primary inductance with Ns2 short

$L_{s1} = L_{KS1} + \frac{L_m}{n^2}$, measure secondary Ns1 inductance with all windings open

$L_{s2} = L_{KS2} + \frac{L_m}{n^2}$, measure secondary Ns2 inductance with all windings open

To simplify calculation, assume Ns1 and Ns2 are symmetric and have identical magnetizing inductance and leakage inductance. L_R=L_{R1}=L_{R2}, L_{KS1}=L_{KS2}=L_{KS}, L_{S1}=L_{S2}=L_S.

$$L_R = L_{KP} + \frac{L_m \cdot n^2 \cdot L_{KS}}{L_m + n^2 \cdot L_{KS}}$$

$$L_s = L_{KS} + \frac{L_m}{n^2}$$

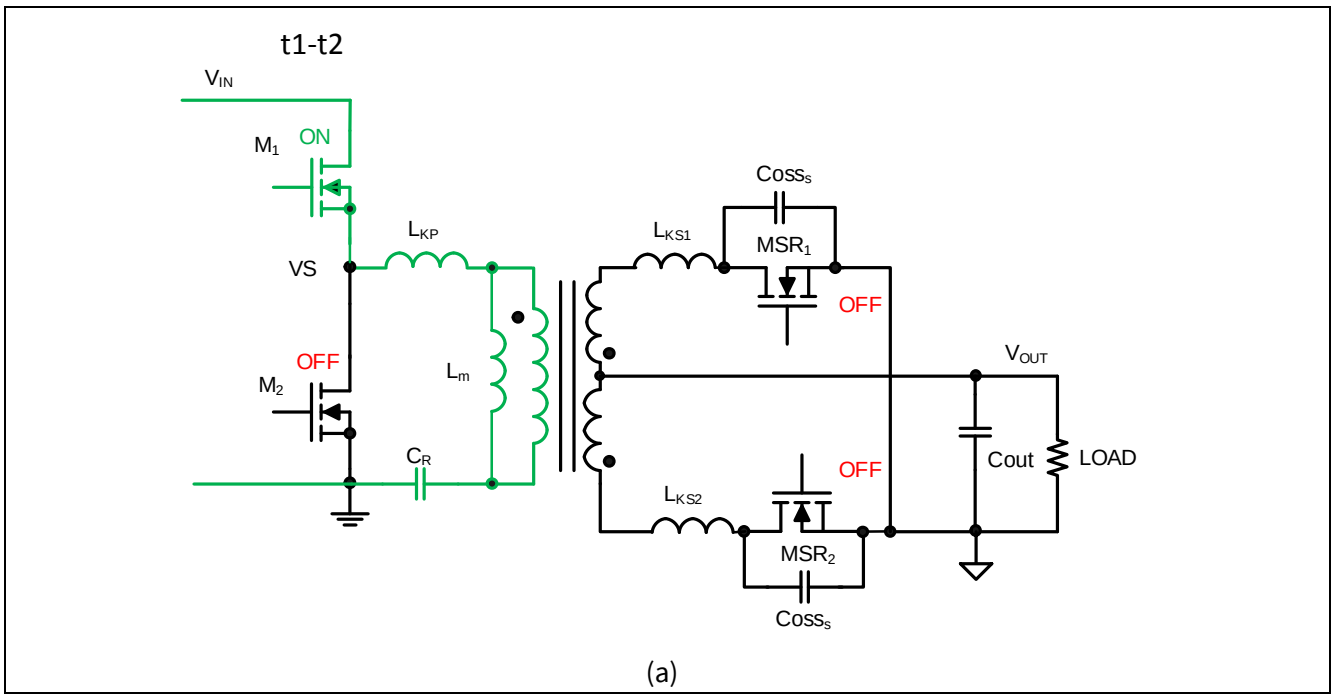
$$L_P = L_{KP} + L_m$$

Three unknowns, three equations, puzzle could be solved. The values could be verified with more measurement. For example secondary leakage inductance can be measured with primary winding Np shorted.

$L_{RS1} = L_{KS1} + \frac{1}{n^2}\frac{L_{KP} \cdot L_m}{L_m + L_{KP}}$, Ns1 leakage inductance measured with Np shorted

Once we have the parameters of a transformer, we can analyze other operation mode. Figure 35 is the equivalent circuit of DCM resonant in t1-t2 interval that mentioned in chapter 5.5. In this mode, both secondary switches are open. Transformer leakage inductor, magnetizing inductor, resonant capacitor C_R and SR MOSFET output capacitor form resonant circuit. The equivalent circuit of transformer is shown in Figure 35(b). The equivalent leakage inductance in this mode can be measured at primary side with both secondary windings shorted.

$L_{R3} = L_{KP} + L_m // (n^2 \cdot L_{KS1}) // (n^2 \cdot L_{KS2})$, primary leakage inductance with Ns1 and Ns2 shorted



(a)

Appendix: Transformer leakage inductance and modeling

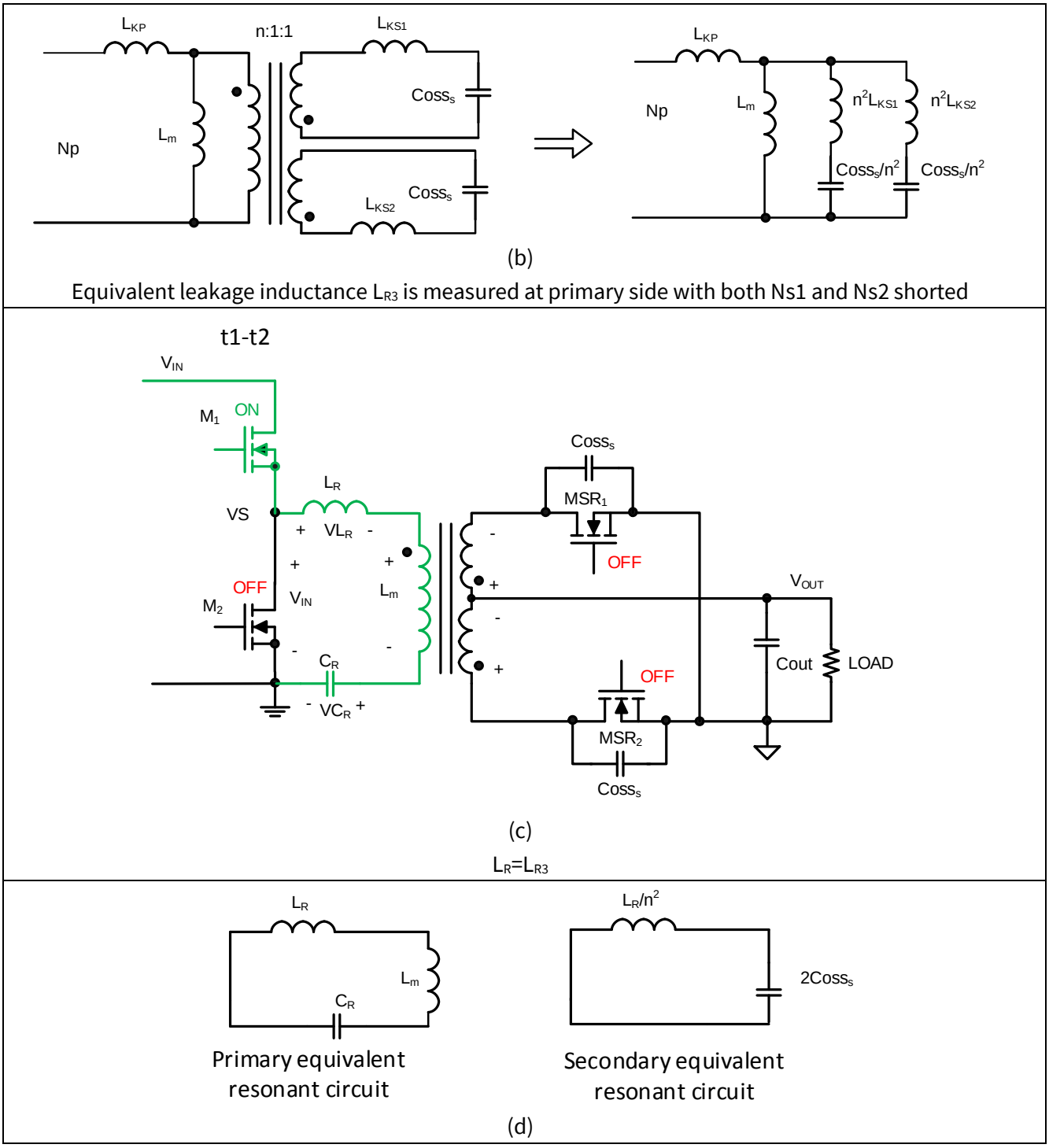


Figure 35 Equivalent transformer model in DCM (t1-t2) of Figure 26

It has two resonant circuits. The first resonant circuit is at primary side: L_R, L_m resonant with C_R at a very low frequency.

$$F_{r2} = \frac{1}{2\pi\sqrt{(L_{R3} + L_m) \cdot C_R}}$$

The second resonant frequency is determined by:

$$Fr3 = \frac{1}{2\pi\sqrt{L_{R3}/n^2 \cdot (2 \cdot Coss_s)}}$$

Appendix: Transformer leakage inductance and modeling

Another important leakage inductance is the leakage between two secondary windings. This leakage inductance can be measured at Ns1 with Ns2 shorted, vice versa. Here name as L_{KS1-2} and L_{KS2-1}. For symmetric secondary, L_{KS1-2} equals L_{KS2-1}. Again this is the total equivalent secondary leakage inductance that physically presents at both Ns1 and Ns2. In the model we could simply split it equally to Ns1 and Ns2. In most conditions, L_{KS1-2} and L_{KS2-1} are too small to affect operation and can be ignored. However, during the turn-off of secondary switch, energy stored in L_{KS1-2} and L_{KS2-1} create voltage spike on V_{DS} of SR MOSFET. It is necessary to have L_{KS1-2} and L_{KS2-1} available for switching loss calculation. Here gives the example of MSR1.

$$P_{SW} = \frac{1}{2} L_{paras} \cdot I_{t3}^2 \cdot f_{sw}$$

$$L_{paras} = L_{KS1-2} + L_{stray} + L_{PCB}$$

$$Fr4 = \frac{1}{2\pi\sqrt{L_{paras} \cdot Coss_s}}$$

L_{stray} is SR MOSFET package inductance, L_{PCB} is PCB trace inductance, I_{t3} is the current in MSR1 at time t3 (Figure 26, Figure 29).

Based on above, we know the equivalent leakage inductance of LLC transformer is not a constant value. It varies with operating mode. Resonant frequency should be calculated with the corresponded leakage inductance in that specific mode.

8 Appendix: Symbols list

Symbols list [1]

V_{TH1}: IR11688 turn-off threshold
V_{TH2}: IR11688 turn-on threshold
V_{TH3}: IR11688 periodic logic (reset) threshold
V_{THR}: IR11688 turn-off regulation threshold
T_{Don}: IR11688 turn on propagation delay
T_{Doff}: IR11688 turn off propagation delay
R_{DSon}: synchronous rectifier MOSFET channel ON resistance
I_D: synchronous rectifier MOSFET drain current
V_{DS}: synchronous rectifier MOSFET drain to source voltage
MOT: IR11688 minimum ON time parameter
t_{blank}: IR11688 turn off blanking time
C_{dc}: IR11688 decoupling capacitor on Vcc
$R_{g1, 2}$: SR MOSFET gate drive loop resistance external to IR11688 IC
R_{CC}: supply voltage series resistor value (Vsupply to V_{CC})
f_{sw}: converter switching frequency
$f_{sw,max}$: converter maximum operating switching frequency
Q_g: SR MOSFET total gate charge
Q_{gd}: SR MOSFET gate to drain (Miller) charge
Q_{gs}: SR MOSFET gate to source charge
L_g: total gate loop parasitic inductance
C_{iss}: SR MOSFET input capacitance
V_m: Miller plateau voltage of MOSFET
C_{sync}: SR MOSFET equivalent input capacitance in ZVS mode
P_{dr}: Total power dissipated by the gate drive function for each SR MOSFET
R_{Source}: gate driver source resistance
R_{Sink}: gate driver sink resistance
P_{Rg}: Power dissipated in each gate resistor
P_{IC}: IR11688 IC maximum power dissipation
V_{CC}: Supply voltage on IR11688 Vcc pin
I_{CC}: IR11688 IC supply current
L_R: LLC resonant inductance
C_R: LLC resonant capacitor
n: transformer turns ratio

[1] IR11688 SmartRectifier™ control IC datasheet

Revision History

Major changes since the last revision

Page or Reference	Description of change
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